

VDKTE

Rosetta 10ADT/10ADTG

LA-9869P REV 1.0 Schematic

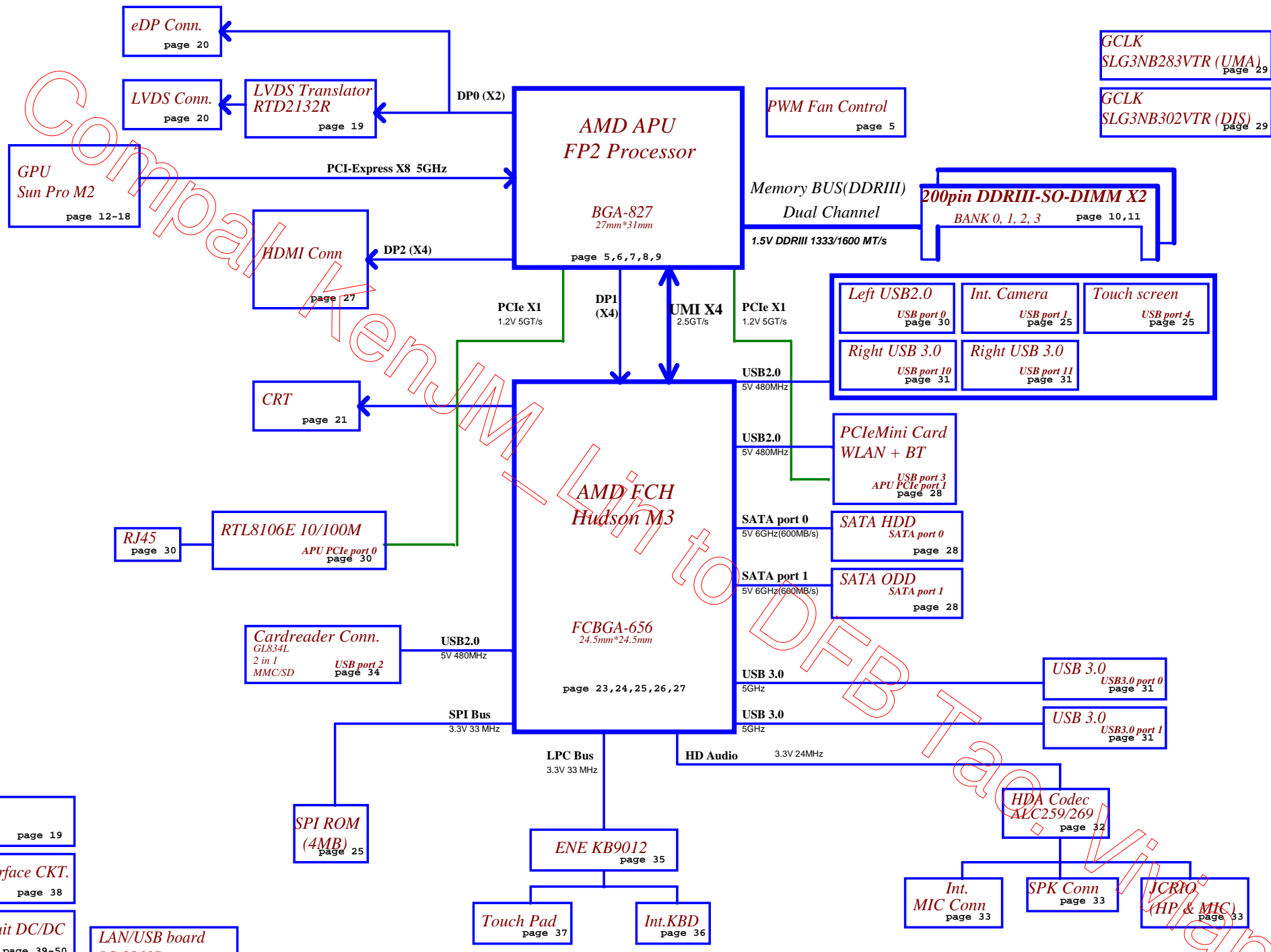
AMD APU RICHLAND FP2 / FCH BOLTON-M3

Sun Pro M2

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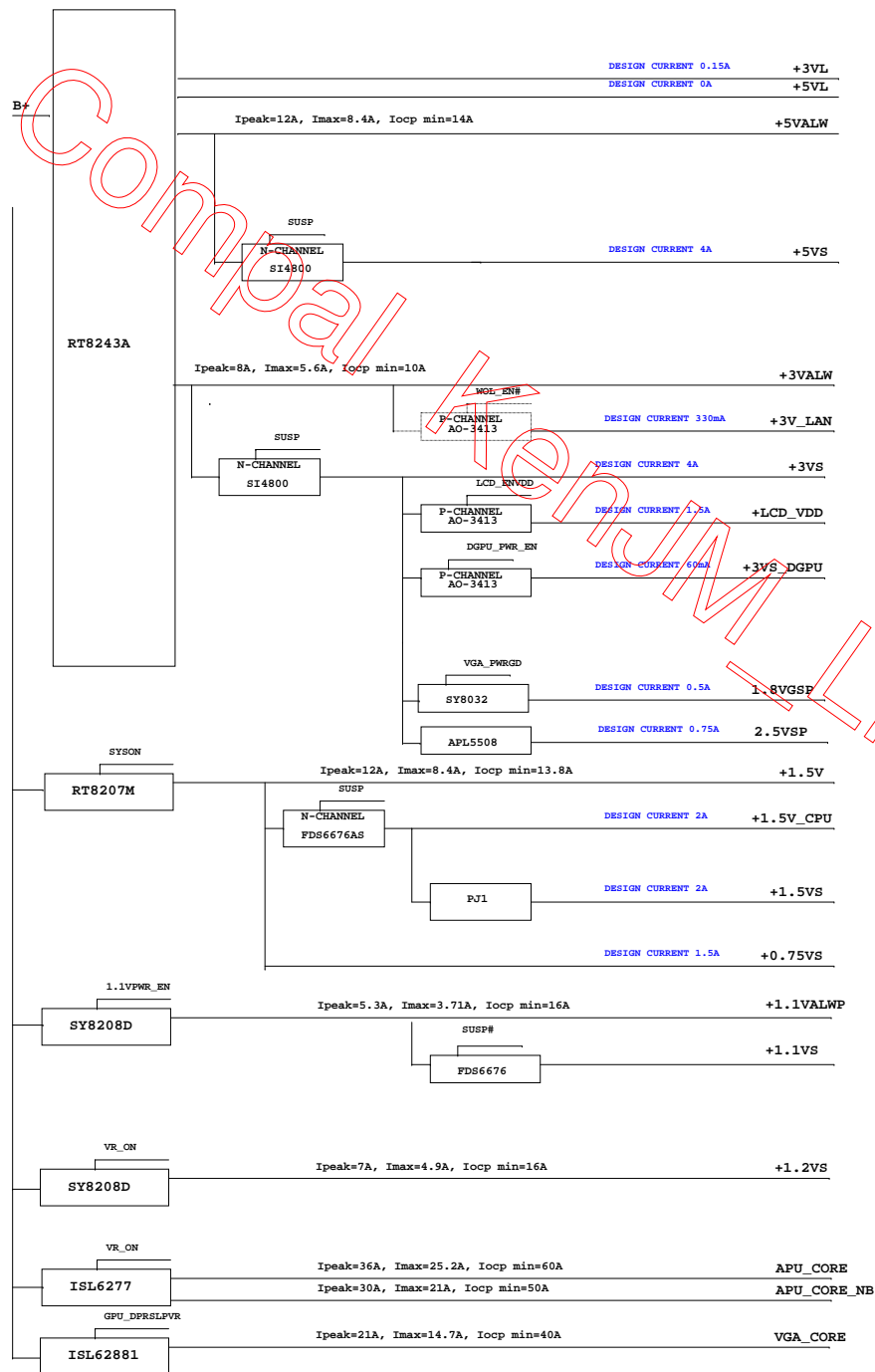
2013-03-20 Rev 1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +1.1VALW
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	APU		FCH		GPU	
description			Bolton			
explain	R1	R3	R1	R3	R1	R3
BTO			BOLTONR1@	HUDM3R3@		

Function	3D sensor	KB LED	Clock		UMA/DIS	
description		K			1G	U
explain	G-sensor	KB LED	Green Clock	No Green Clock	DIS	UMA
BTO	GSSENSOR@	KBL@	GCLK@	NOGCLK@	VGA@	UMA@

Function	Panel			
description	S	D		
explain	LVDS	eDP		
BTO	LVDS@	IEDP@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b

EC SM Bus2 Address

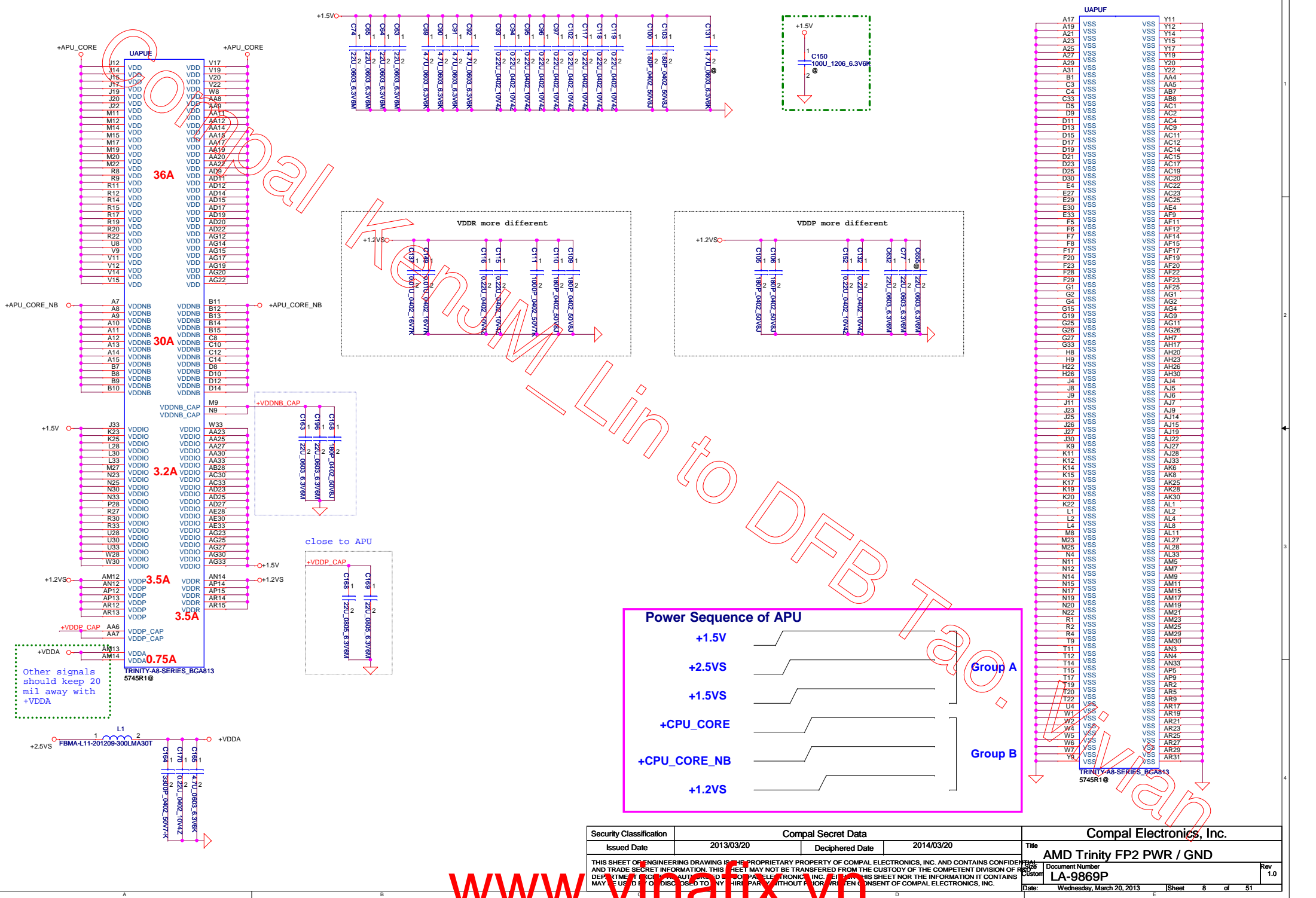
Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	VGA Thermal	82H	1000 0010 b

EC SM Bus3 Address

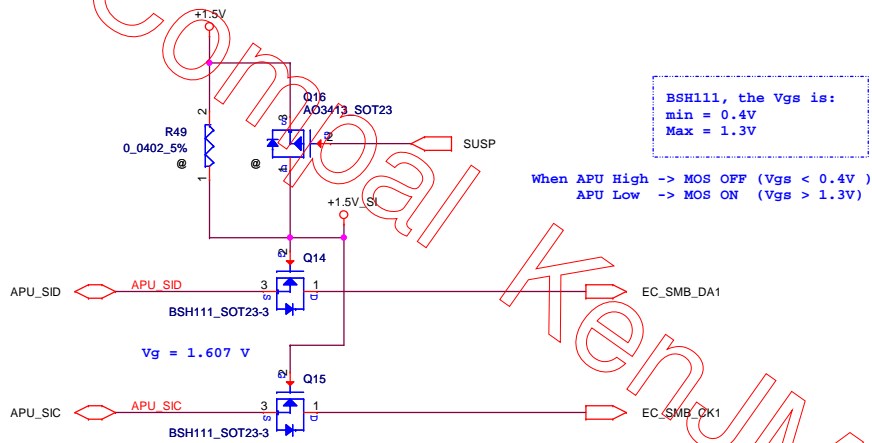
Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

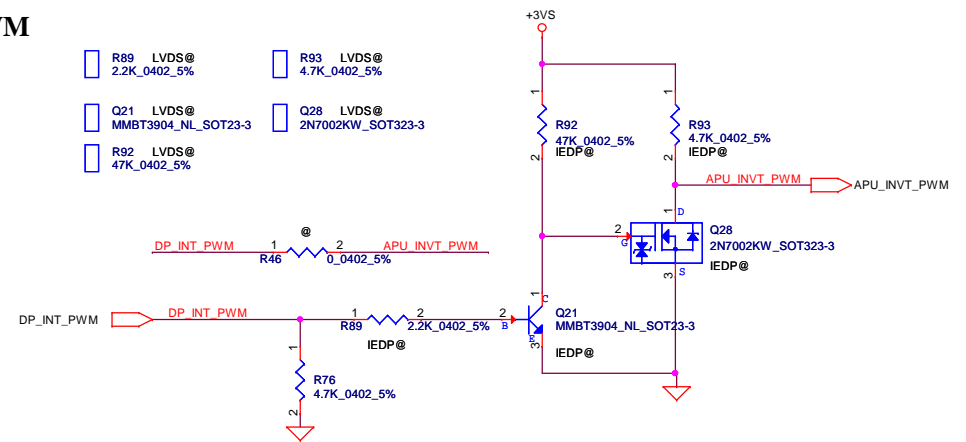
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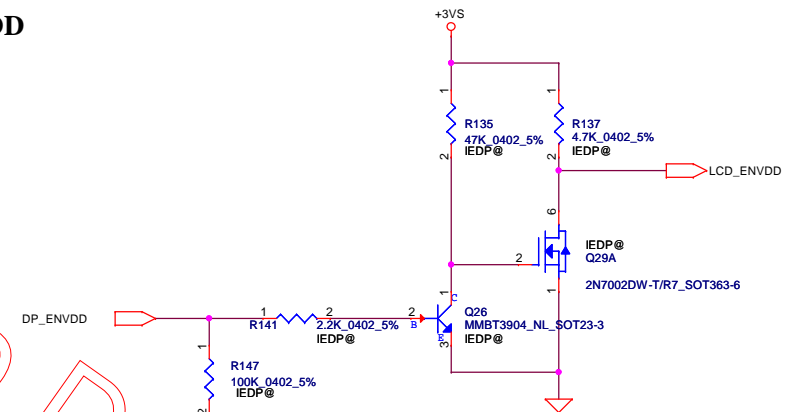
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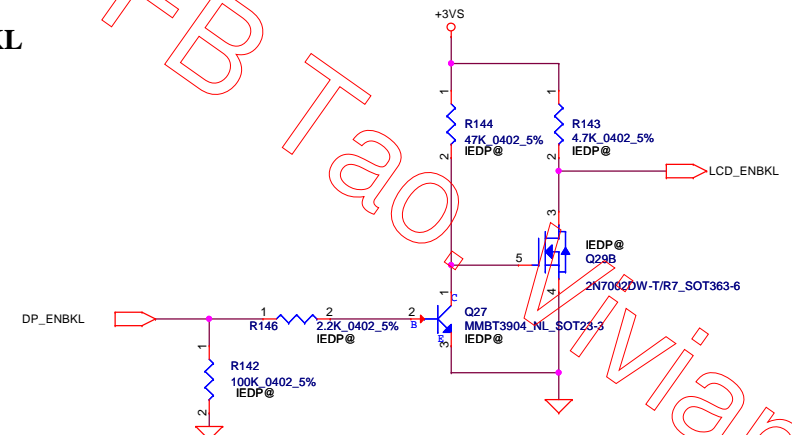
Panel PWM



eDP Panel ENVDD



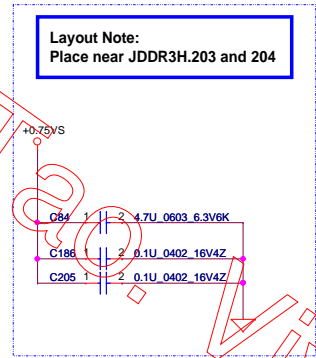
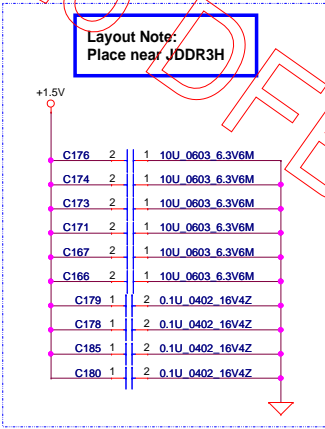
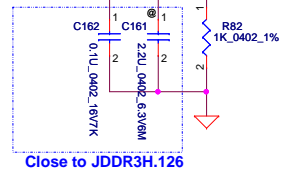
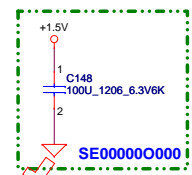
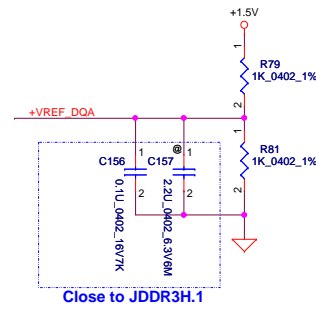
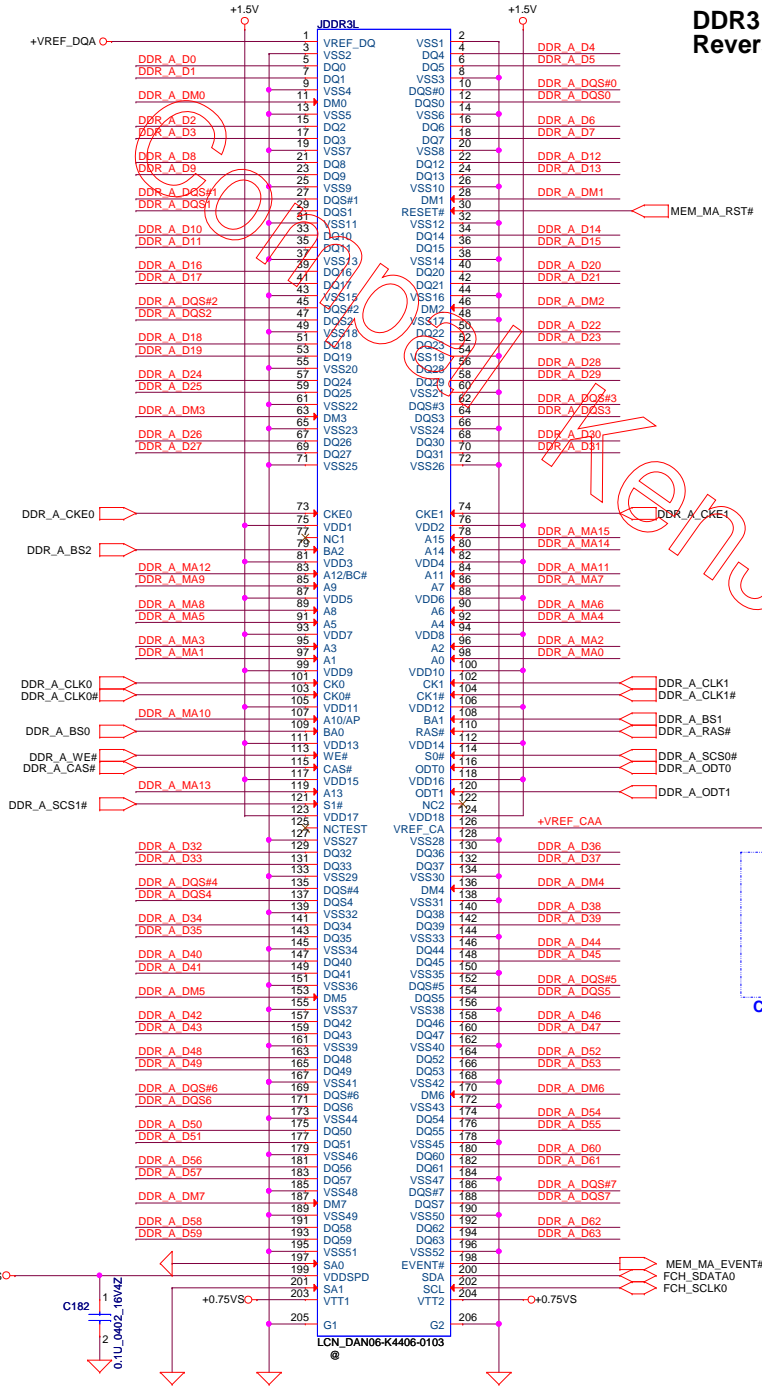
eDP Panel ENBKL



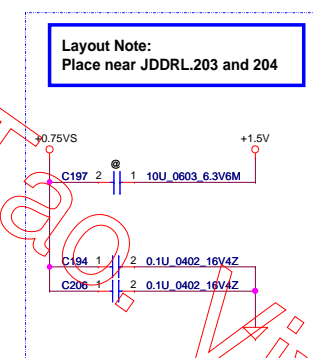
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				AMD Trinity FP2 Singal Level Shifter					
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DDR3 SO-DIMM A Reverse Type

- DDR_A_DQS[0..7]
- DDR_A_DQS#[0..7]
- DDR_A_DQ[0..63]
- DDR_A_MA[0..15]
- DDR_A_DM[0..7]



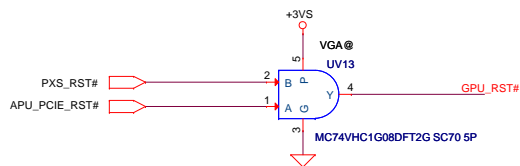
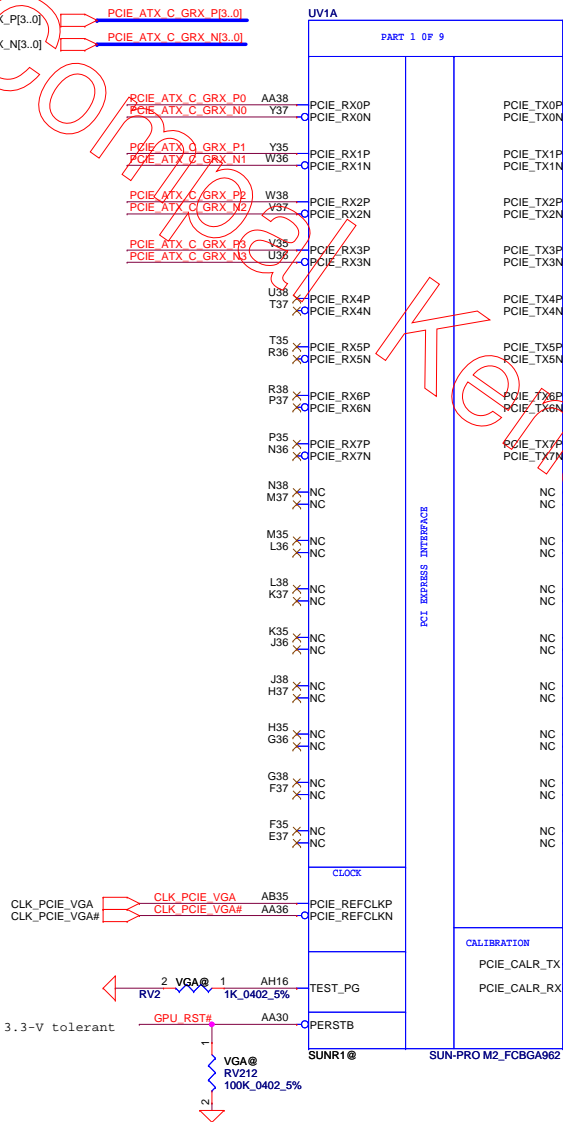
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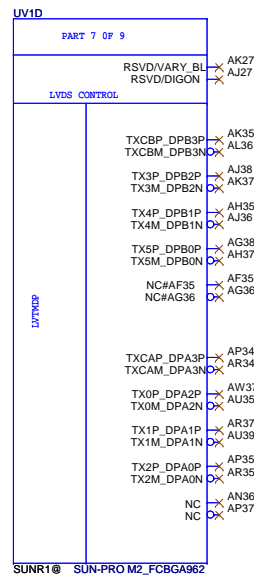
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PCIE_ATX_C_GRX_P[3..0] PCIE_ATX_C_GRX_P[3..0]
PCIE_ATX_C_GRX_N[3..0] PCIE_ATX_C_GRX_N[3..0]

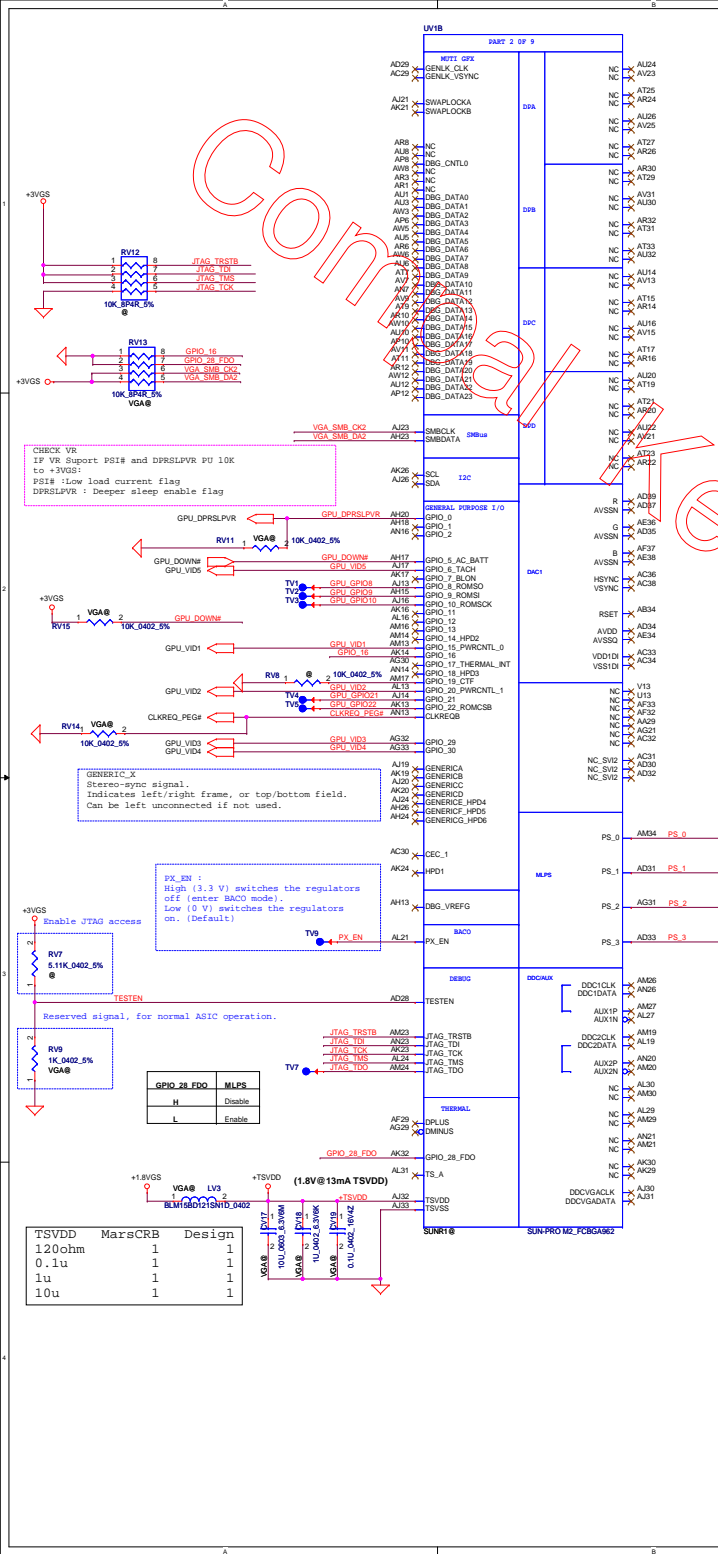
PCIE GTX_C_ARX_P[3..0] PCIE GTX_C_ARX_P[3..0]
PCIE GTX_C_ARX_N[3..0] PCIE GTX_C_ARX_N[3..0]



LVDS Interface



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								PCIE/LVDS	
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Primary Memory Aperture Size Requested at PCI Configuration			
Size of the Primary Memory Apertures	ROM_CONFIG [2:0]		
128 MB	000		
256 MB	001		
64 MB	010		
Reserved	011		
512 MB	Not supported		
1 GB	Not supported		
2 GB	Not supported		
4 GB	Not supported		

Mars MLPS configuration			
Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Pin Name	Type	PD/PU	Description
GPIO_0	I/O	PD-reset	Power-state indicator. Penalty for voltage regulator to activate power-saving features. If V8 support PS1# and DPRSPLVR PU 10K to +3VGS. PS1# : Low load current flag DPRSPLVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O	PD-reset	(Optional) An input which allows the system to request a <i>partial power reduction</i> by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disrupt the display momentarily. Power reduction must any time <i>cpu0</i> should use the standard software methods in order to prevent display disturbances.
GPIO_6	I/O	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be forced to a weak internal pull-down resistors. The VDDC can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Notes: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_10_ROMSD	I	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, no use the test point.
GPIO_9_ROMSI	I	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK	O	PD-reset	Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB	I	PD-reset	BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, no use the test points.
GPIO_17_THERMAL_INT	I/O	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb). Critical temperature fault (CTP) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTP setpoint is 109°C by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_19_CTP	O	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_21	I/O	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
GPIO_28_FDO	I/O	PD-reset	Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC. On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PU is asserted and PERSTb is deasserted.
CLKREQB	O		
PX_EN	O	PD	

MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1]	ROM_CONFIG[0]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNCR	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_RIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_RIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter [Tx] power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	RIF_VDA_VDIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1]	BOARD_CONFIG[0]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_3[2]	BOARD_CONFIG[1]	N/A		
PS_3[3]	BOARD_CONFIG[2]	N/A		
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

For MEMCLK 1GHz	brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skhynix	H5TQ2G63DPR-N0C	1.5V/1GHz	000	NC	4750
	Samsumg	K4W201646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skhynix	H5TQ2G63DPR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-1070:K	1.35V-1.5V/900MHz	001	8450	2000
	Samsumg	K4W201646E-MC11	1.5V/900MHz	111	4750	NC

MLPS Strap

Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	001	NC	8.45k 2K
PS_1[5:1]	11	001	NC	8.45k 2K
PS_2[5:1]	00	000	880 nF	NC 475k
PS_3[5:1]	11	XXX	NC	X X

Mapping to VRAM type please refer to page 6

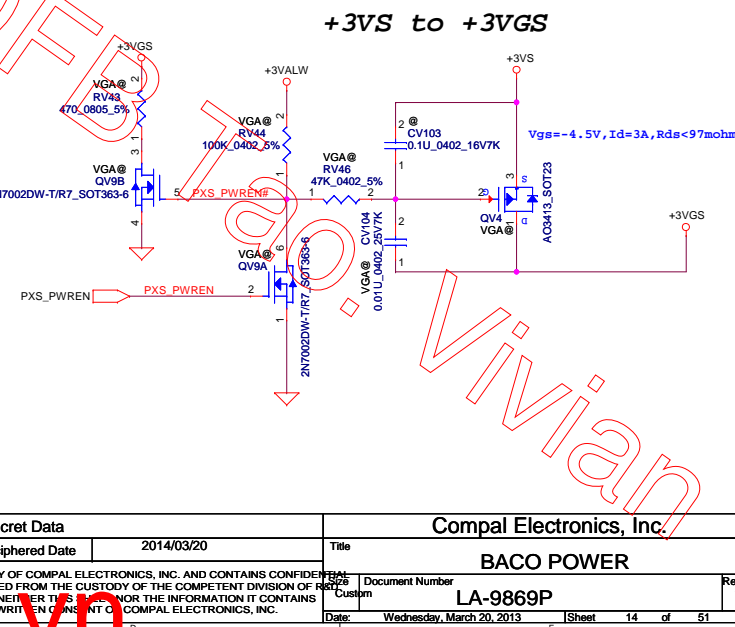
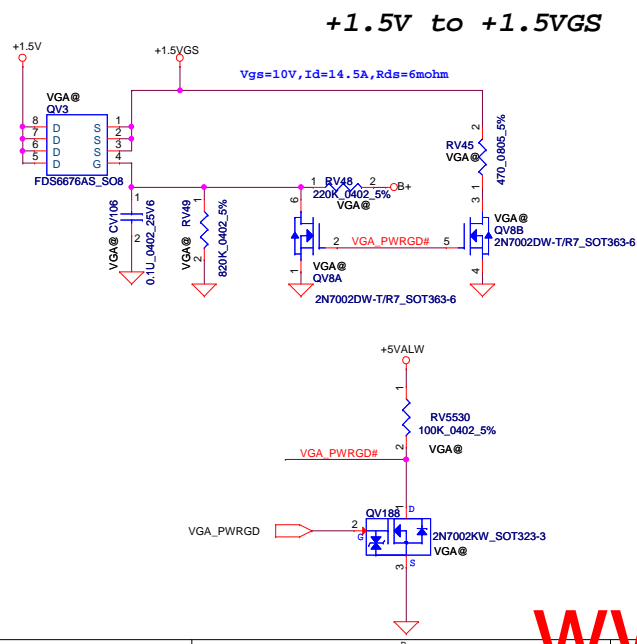
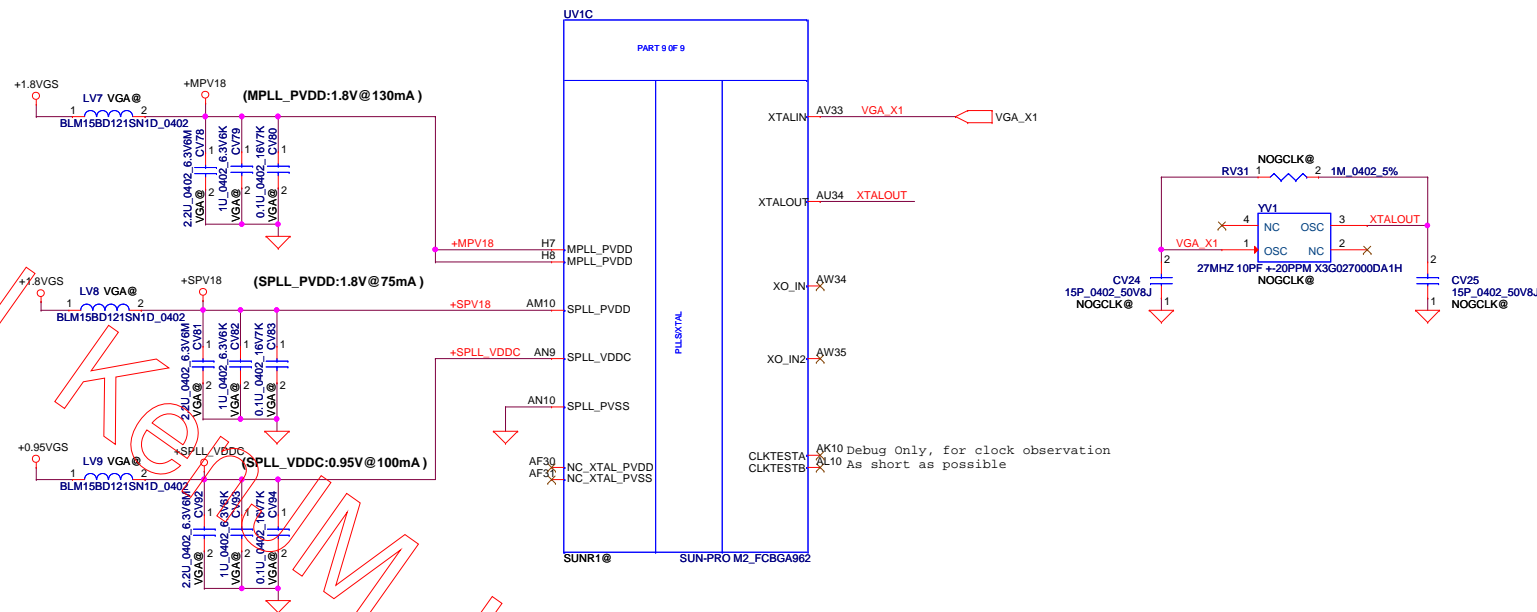
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SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

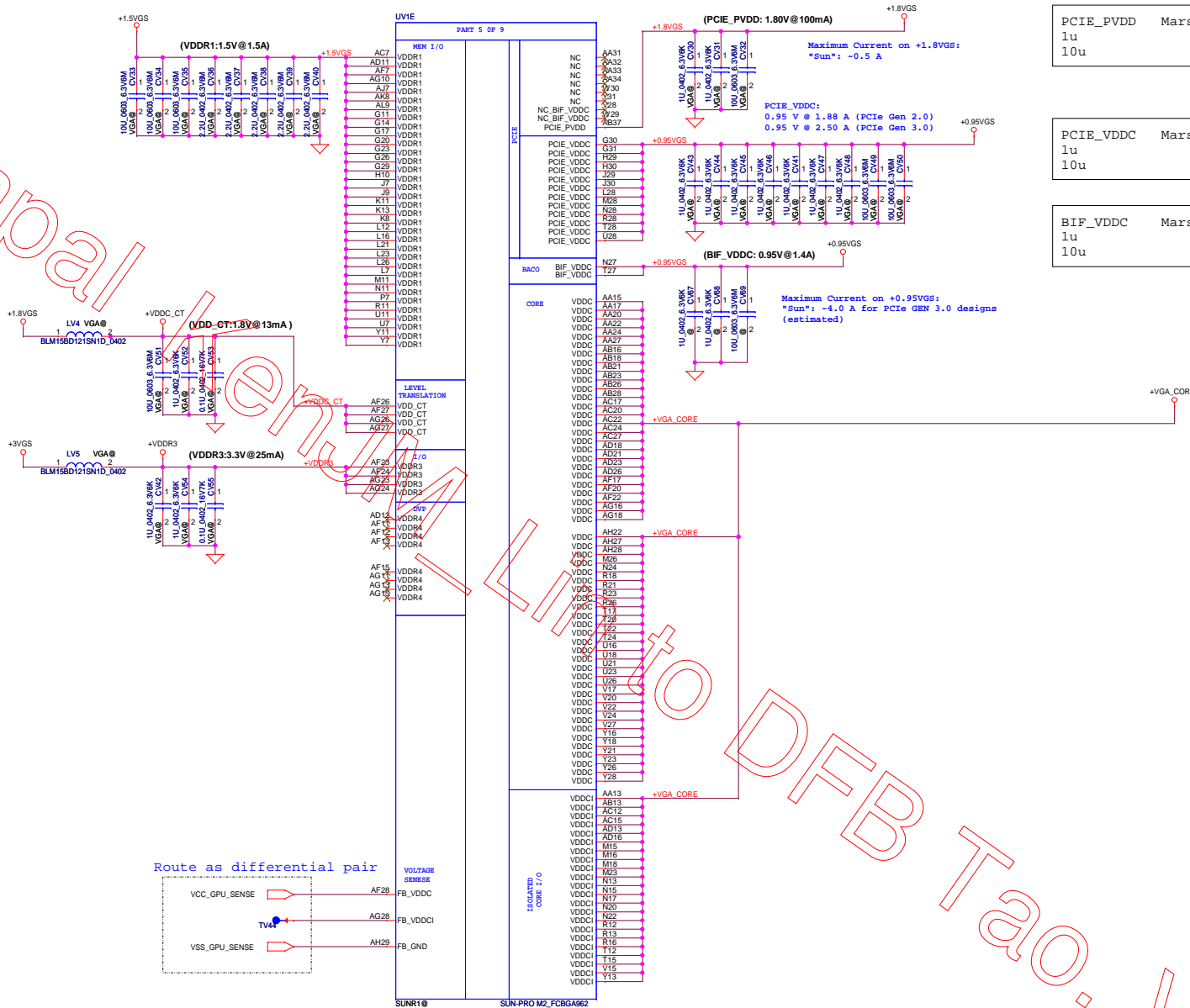


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VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars	check list	Design
120ohm	1		1
1u	3		2
10u	1		0
0.1u	0		1



PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

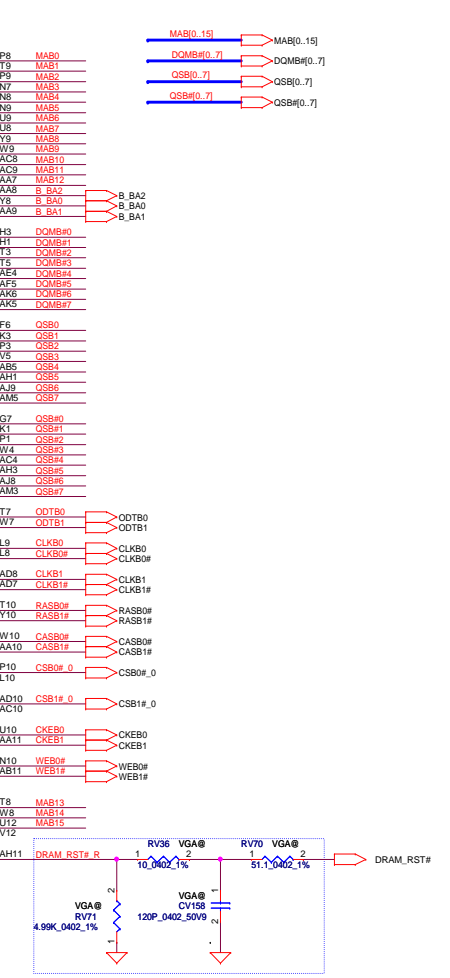
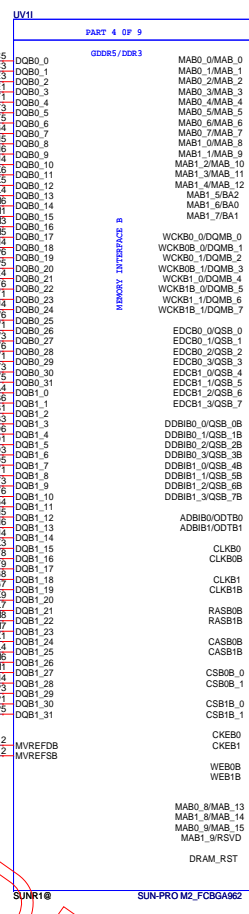
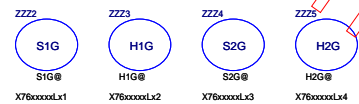
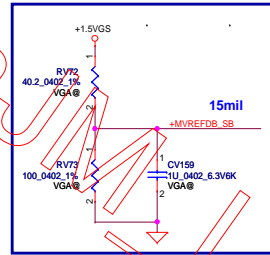
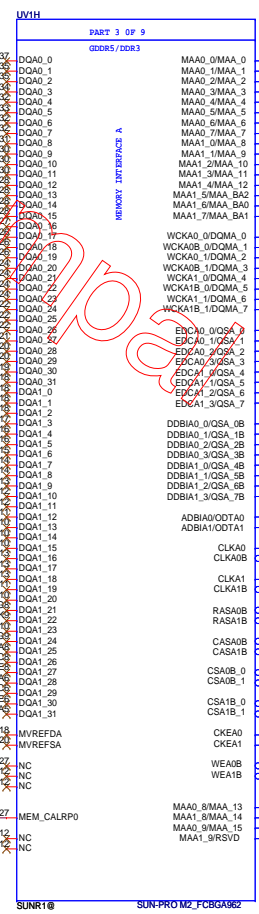
PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

BIF_VDDC	Mars	check list	Design
1u	1		1
10u	1		1

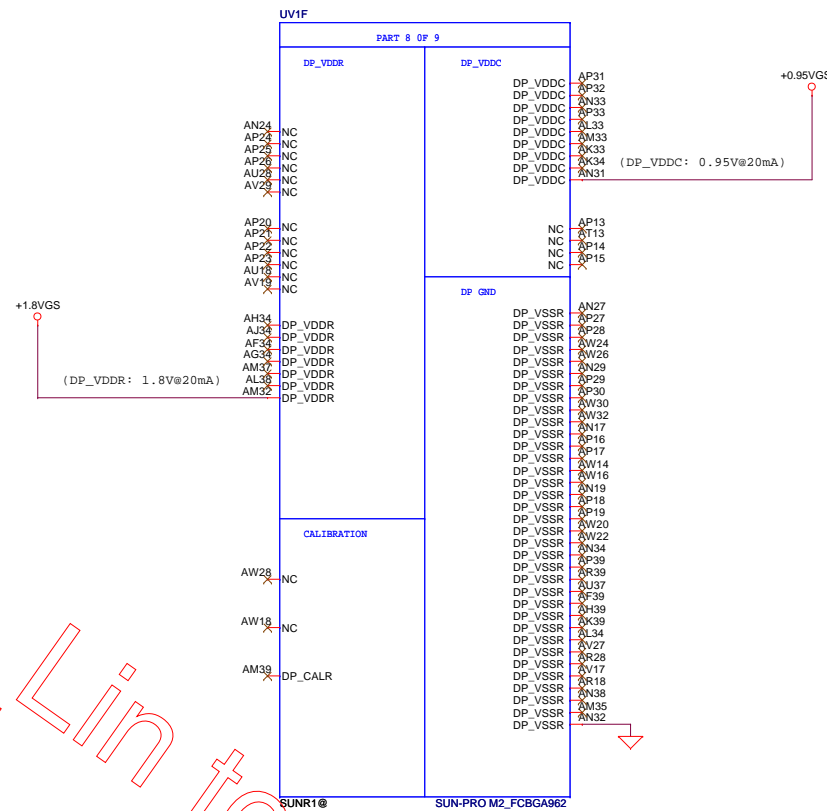
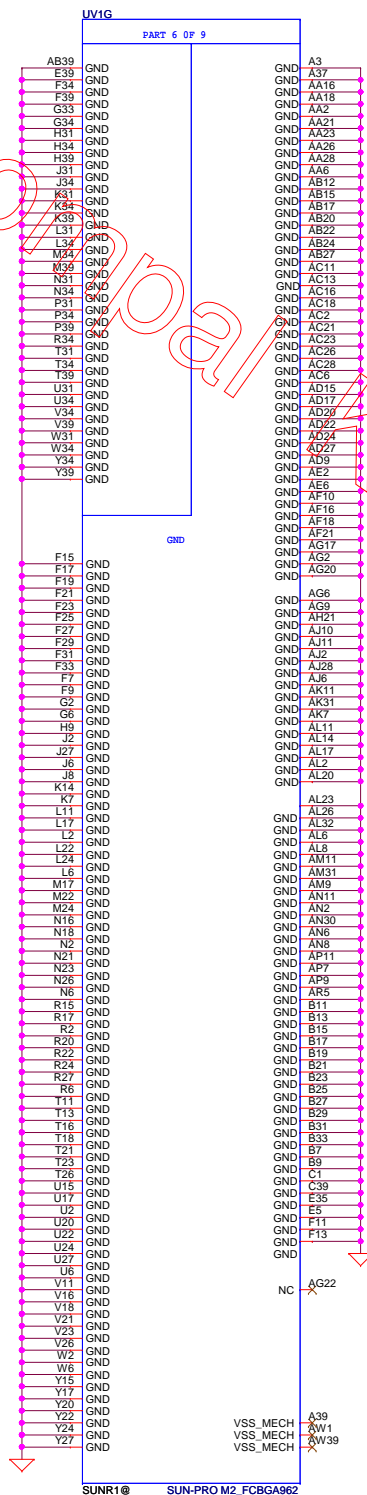
Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

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Power				Power				Document Number			
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1.0				1.0				Date			
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51				51				51			

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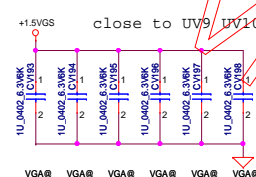
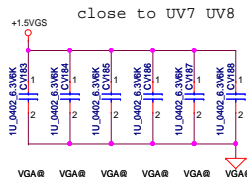
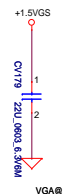
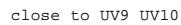


GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YOG0	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Hynix	SA000065320	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M2	64bit	Micron	SA00005XB10	MT41K128M16JT-107G.K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH40	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	0	RV20 3.4K	RV27 10K



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Supported Memory Configurations: Up to 4 Gbit/part for DDR3.

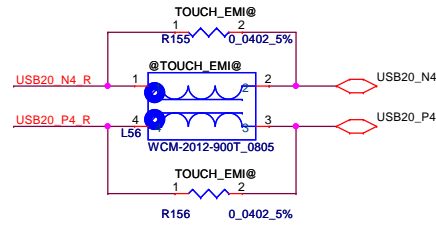
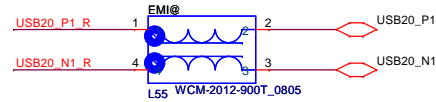
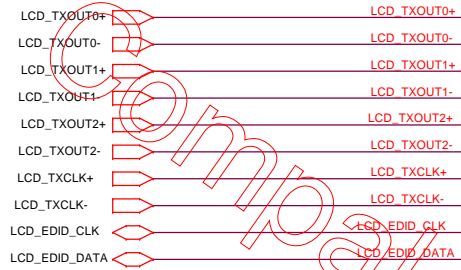


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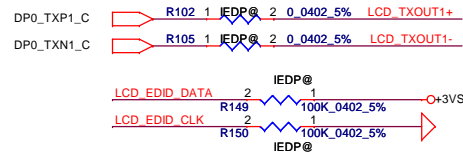
2132R	RT24	
※ If use 2132R, please select LDO mode as default.		



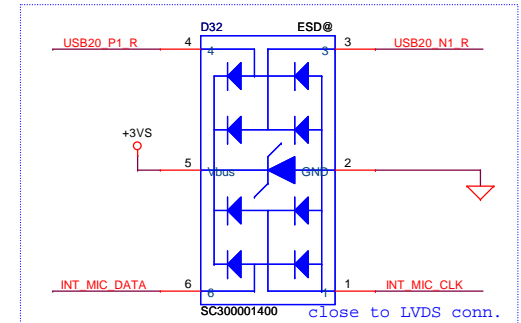
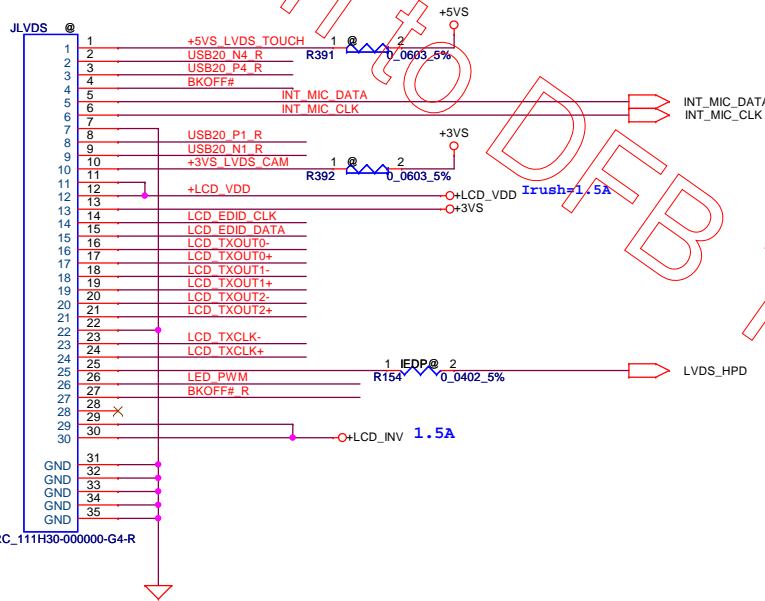
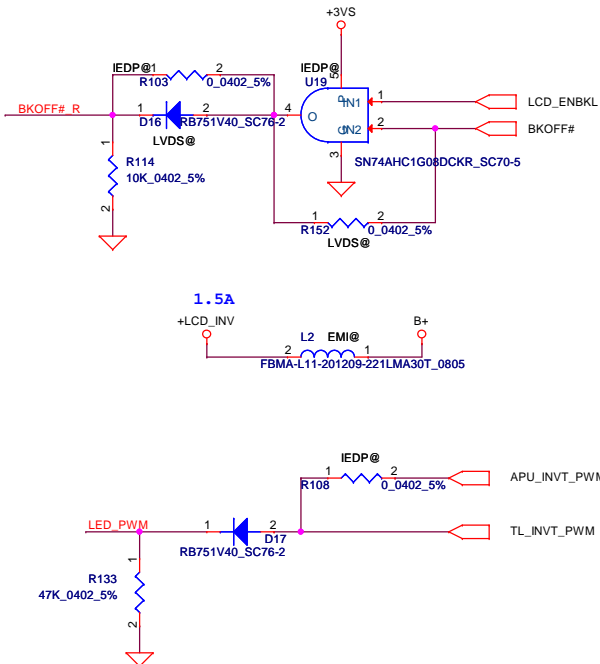
For LVDS 1ch Panel



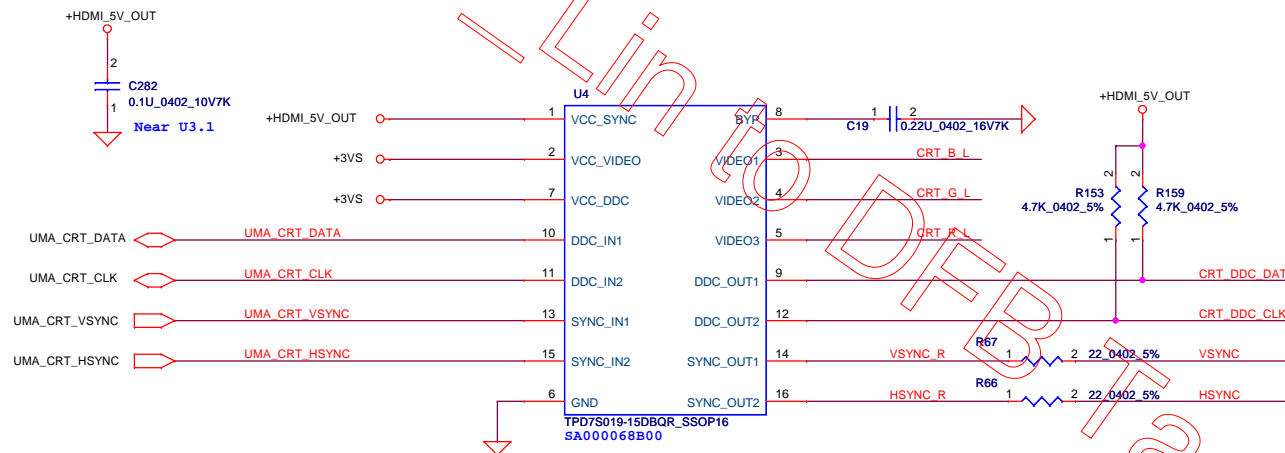
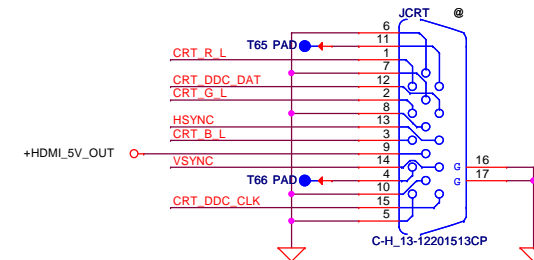
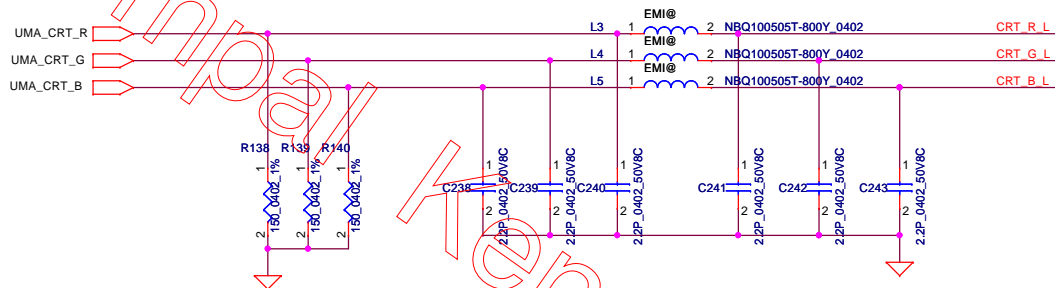
For eDP Panel



Reserve for eDP panel potience issue



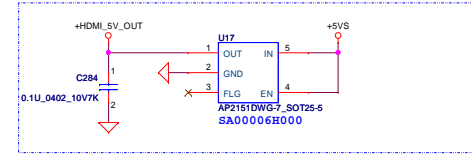
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										Date	
										Wednesday, March 20, 2013	
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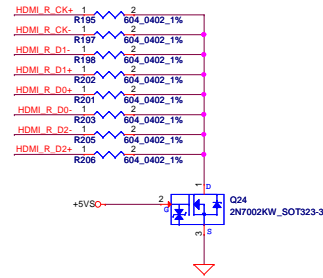
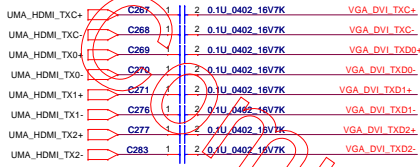
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HDMI POWER CIRCUIT

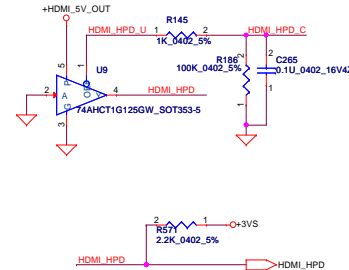
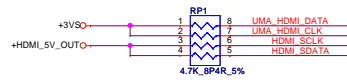
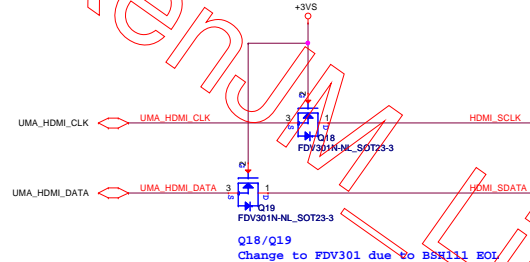
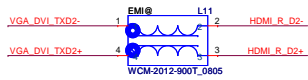
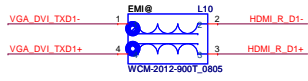
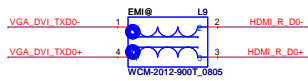
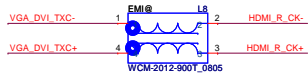
VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



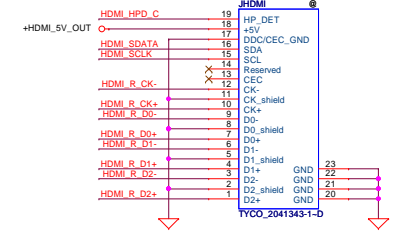
HDMI Royalty
HDMI W/Logo + HDCP
R00000003HM
HDMI W/O Logo: R00000001HM
HDMI W/Logo: R00000002HM
HDMI W/Logo + HDCP: R00000003HM



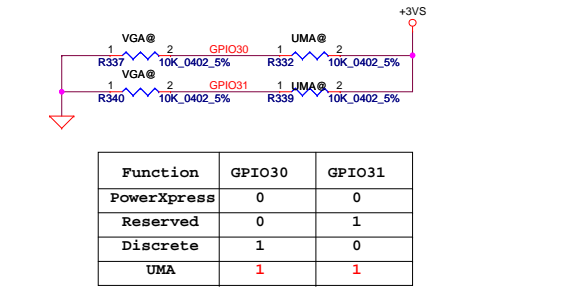
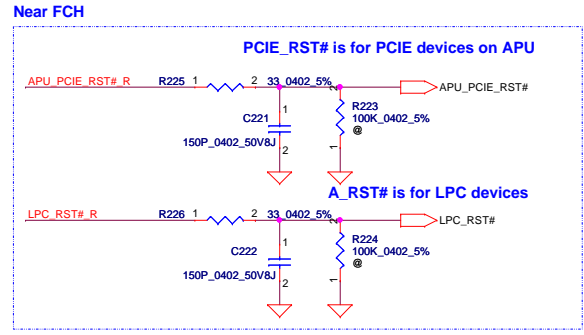
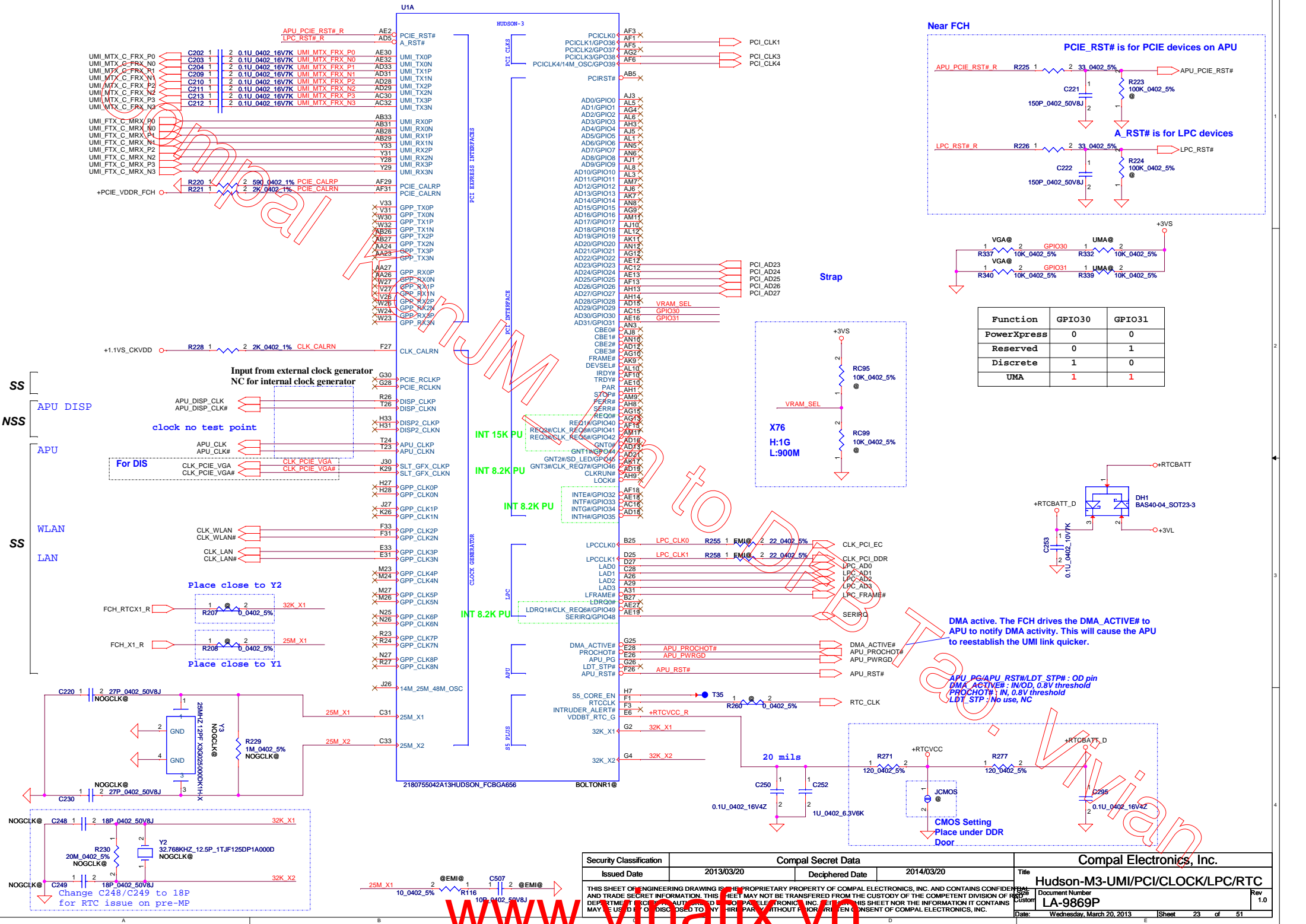
Change R184 and R185 from 2K to 4.7K for HDMI detect issue on Comal



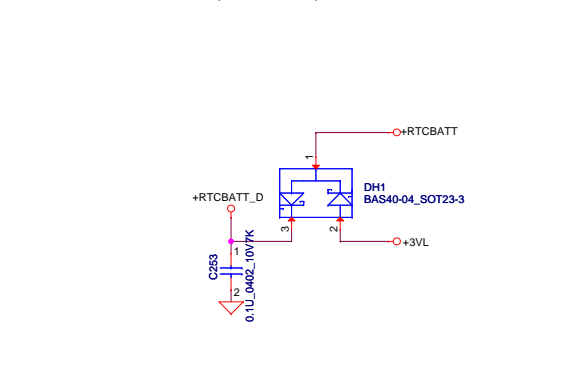
HDMI Connector



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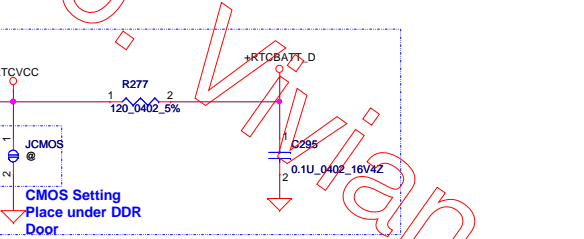


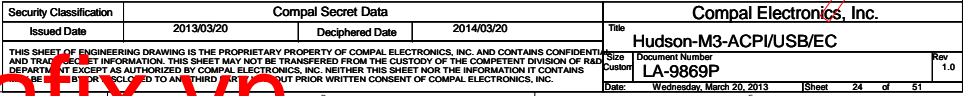
Function	GPIO30	GPIO31
PowerXpress	0	0
Reserved	0	1
Discrete	1	0
UMA	1	1



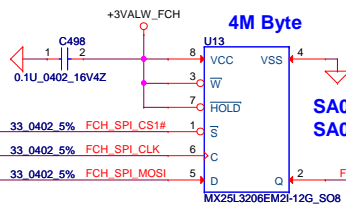
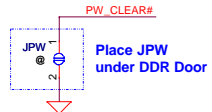
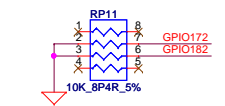
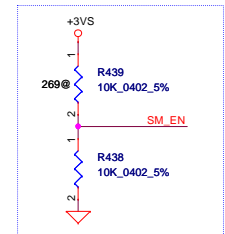
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

APU PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP# : No use, NC

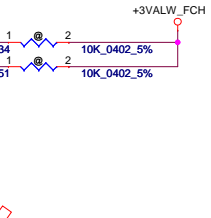
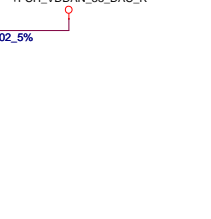
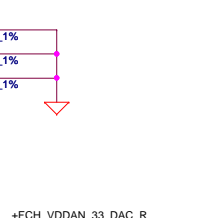
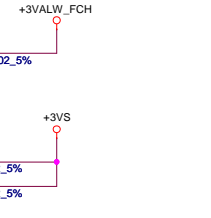
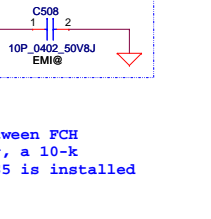
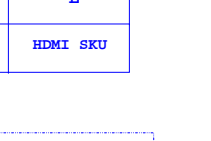
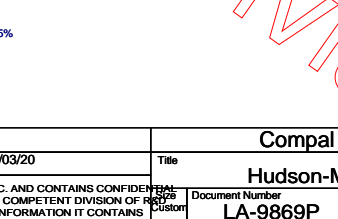
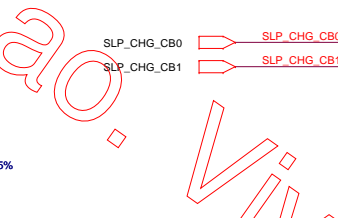
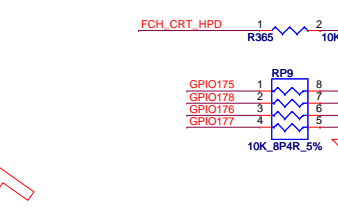
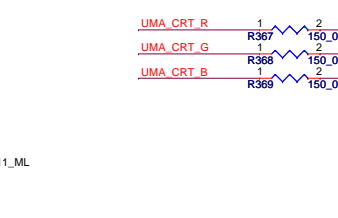
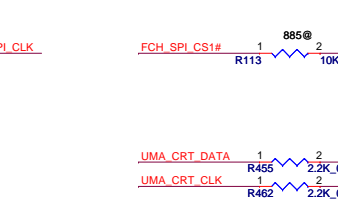
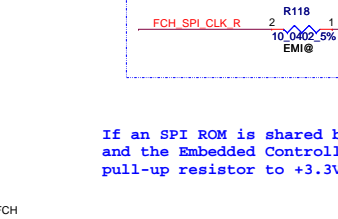
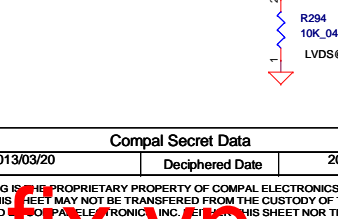
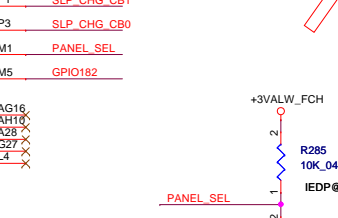
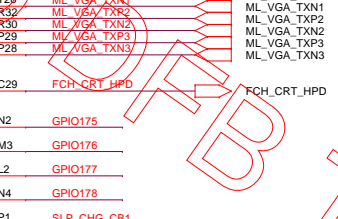
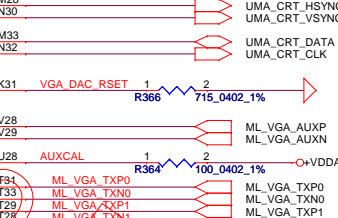
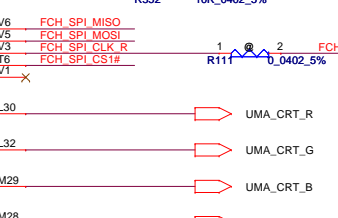
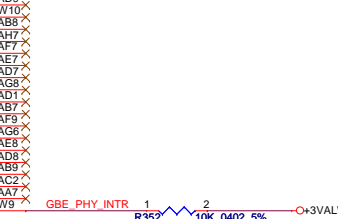
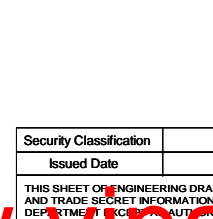
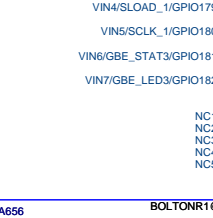
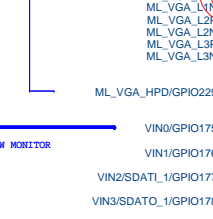
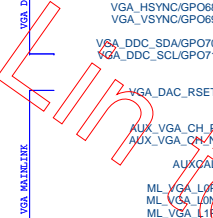
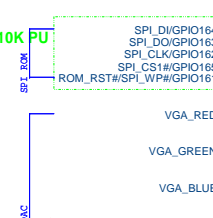
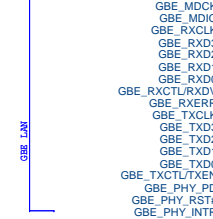
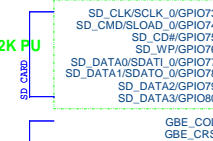
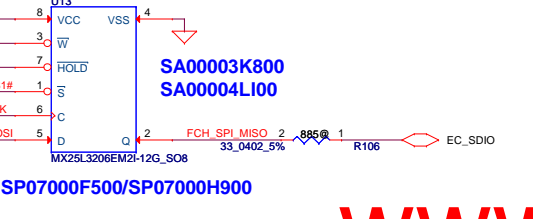
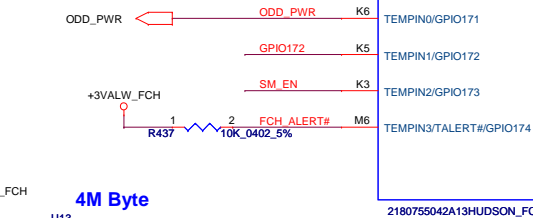
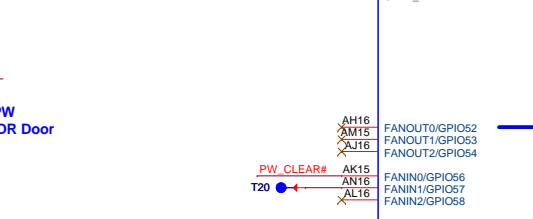
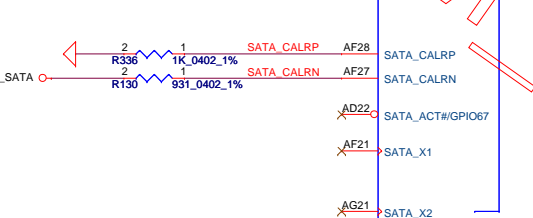
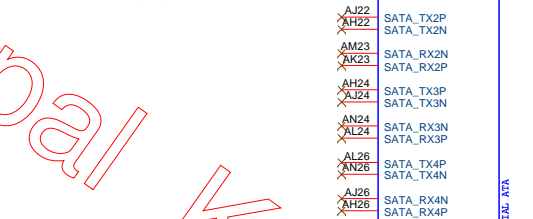




SM_EN	BIOS SETUP	SPK TYPE
1	S&M OPTION	HARMAN KARDON
0	NO	NO HARMAN



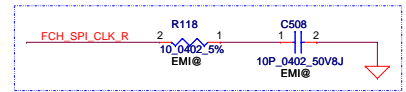
Socket PN: SP07000F500/SP07000H900



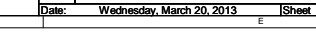
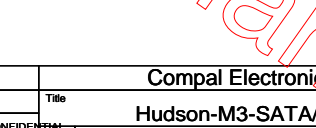
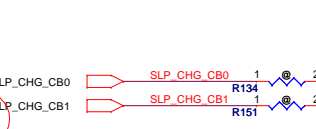
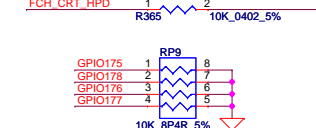
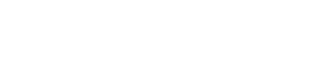
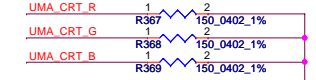
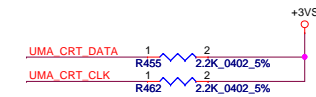
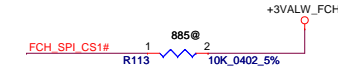
HDMI_EN# (Internal 8.2K PU)

HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

For EMI request



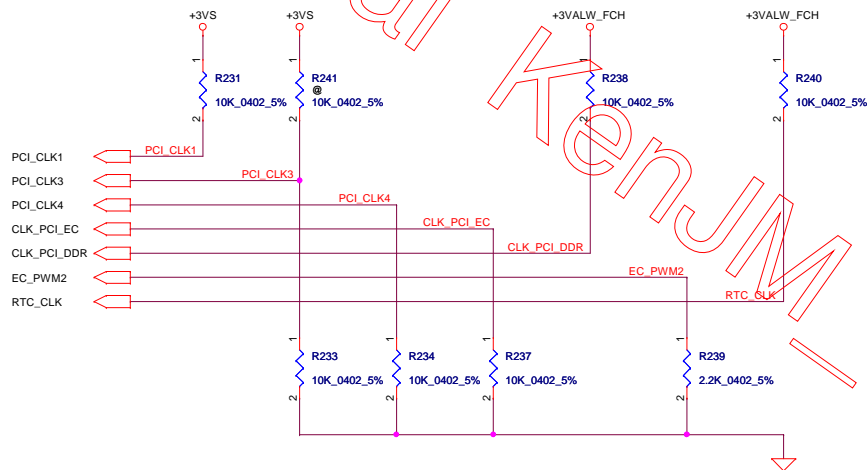
If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed



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STRAP PINS

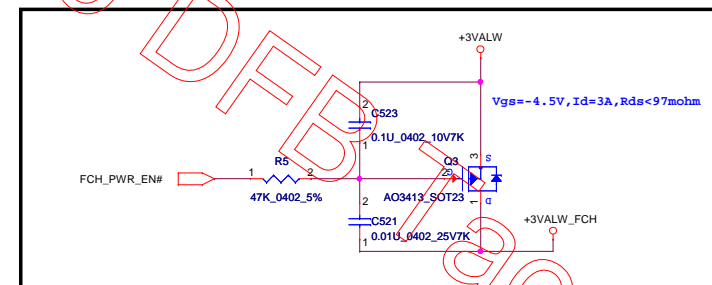
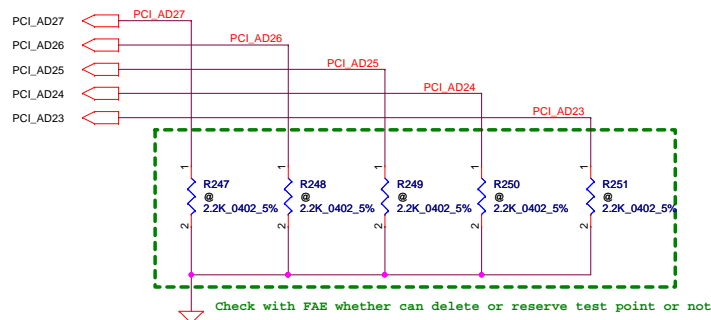
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 (DEFAULT)	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED (DEFAULT)	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED (DEFAULT)
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP (DEFAULT)	FUSION CLOCK MODE (DEFAULT)	EC DISABLED (DEFAULT)	CLKGEN DISABLE	SPI ROM (DEFAULT)	S5 PLUS MODE ENABLED



DEBUG STRAPS

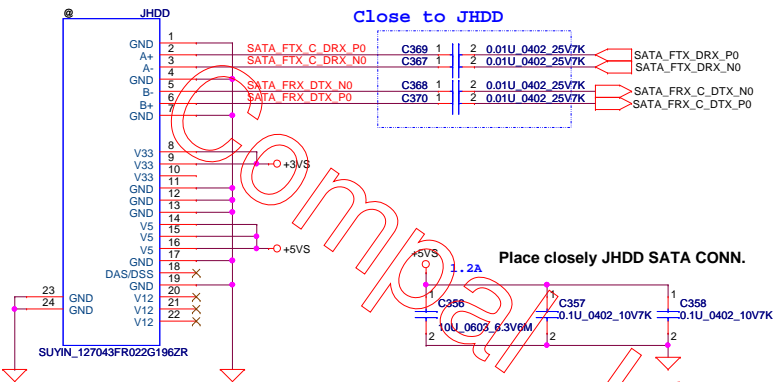
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	DISABLE ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	DISABLE PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

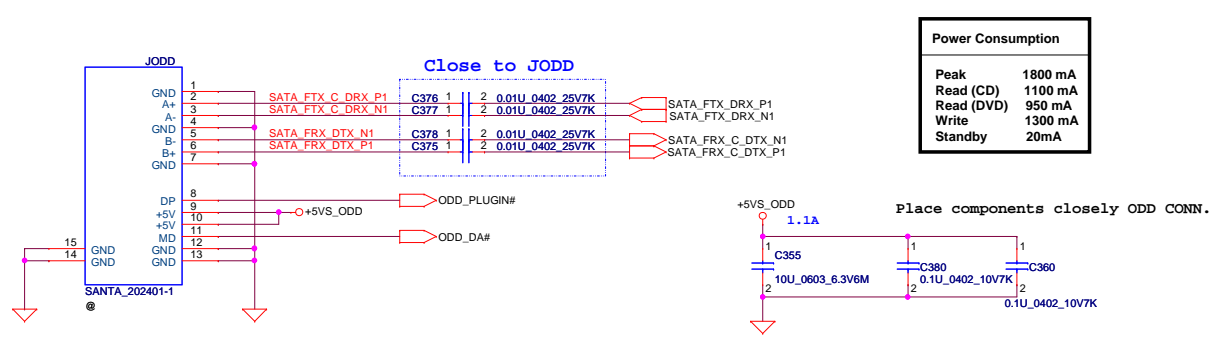


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				Rev 1.0
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SATA HDD Conn.

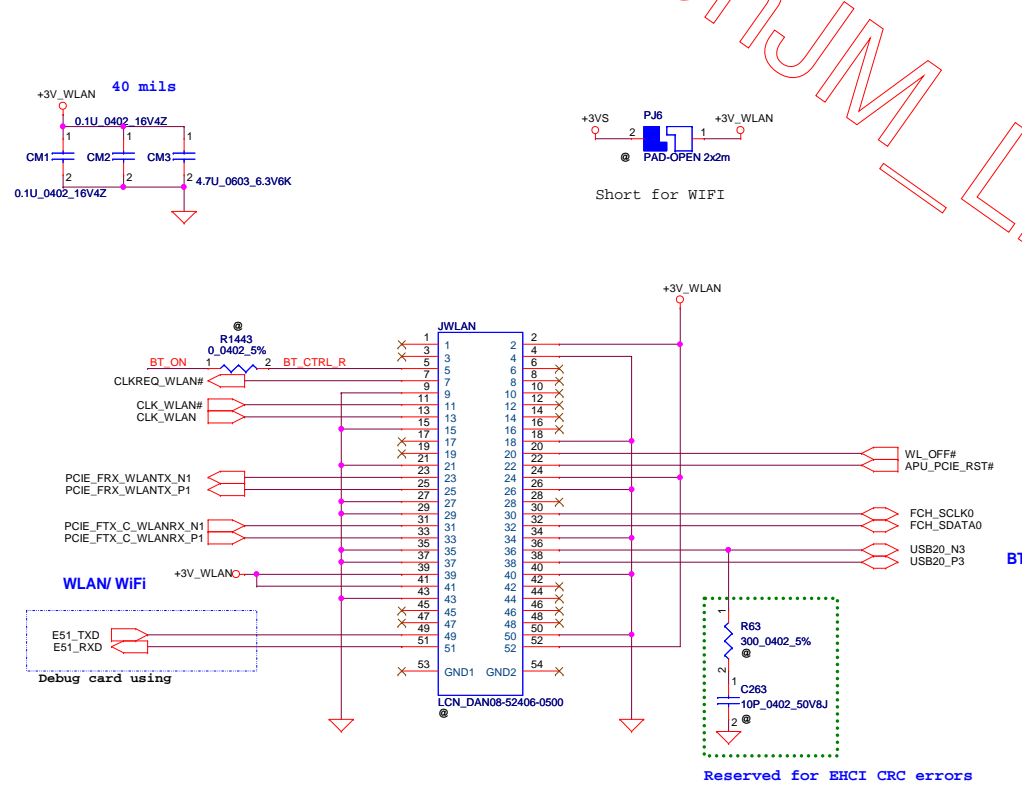


SATA ODD Conn



Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

Slot 1 Half PCIe Mini Card-WLAN



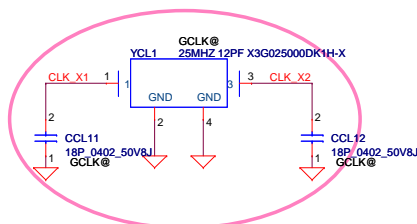
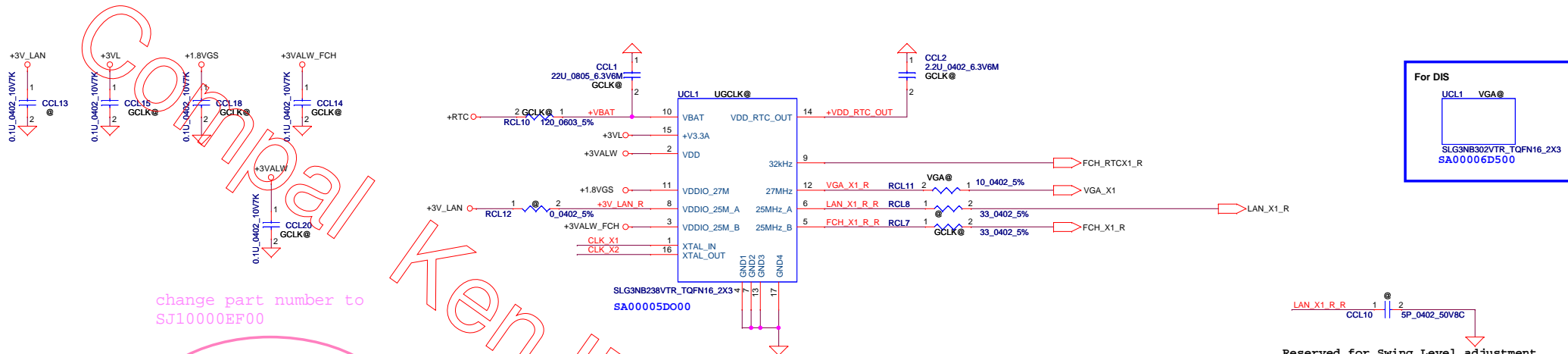
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

BT_ON, BT_ON, R327, E51_RXD, 1K_0402_5%

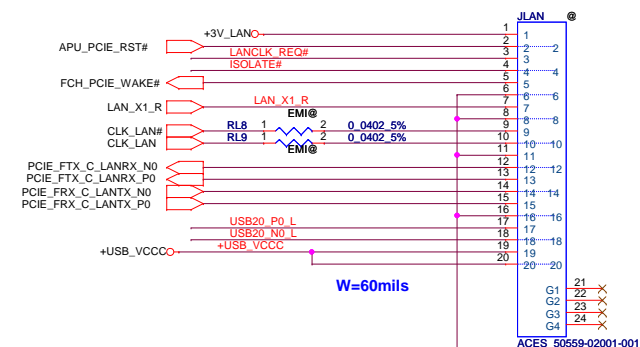
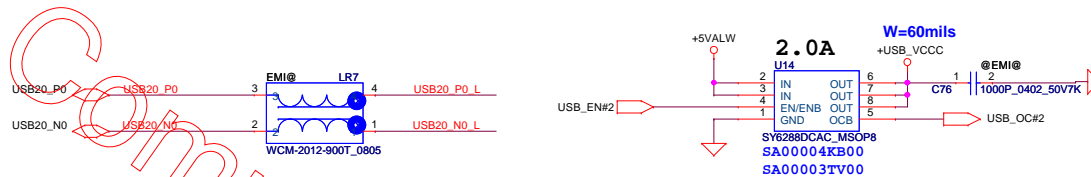
For isolate BT_CTRL and Compal Debug Card.

Green Clock Generator

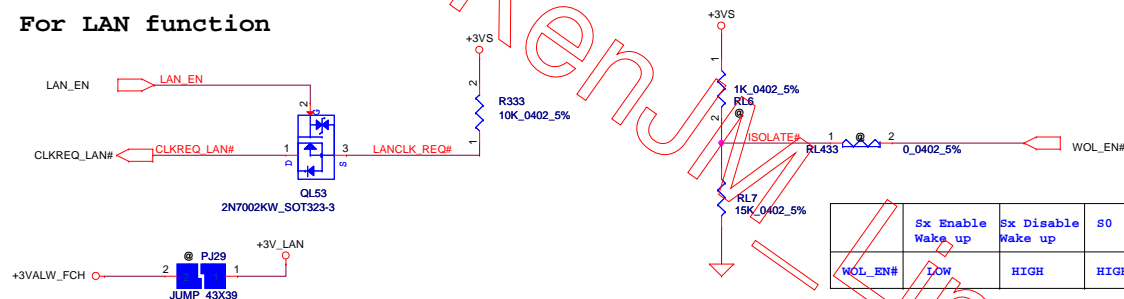


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Issued Date	2013/03/20	Deciphered Date	2014/03/20	PCle-WLAN/GCLK	
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Left USB 2.0 x 1



For LAN function



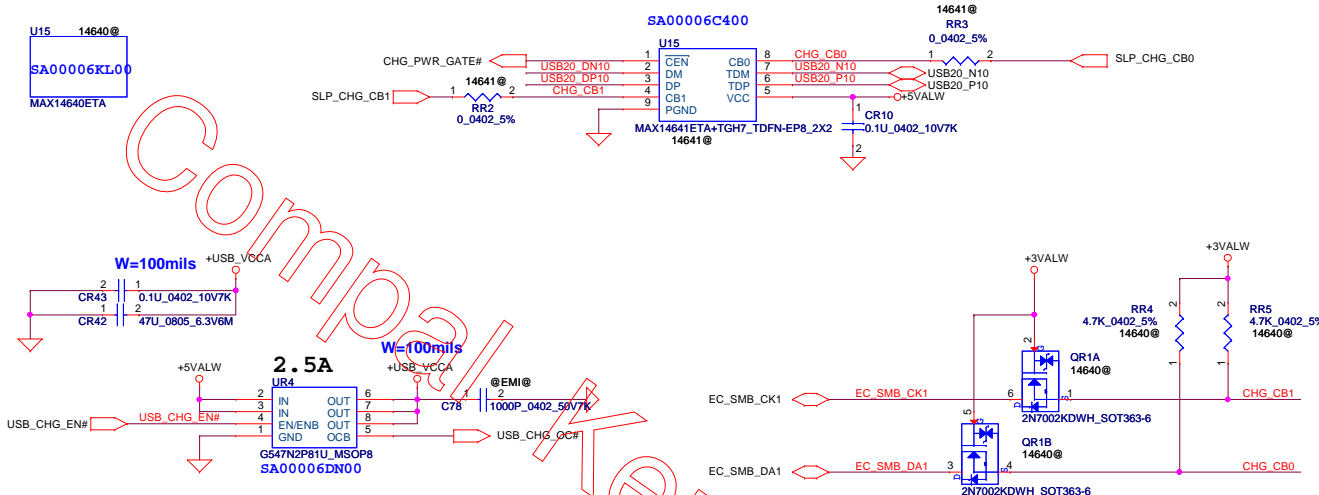
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

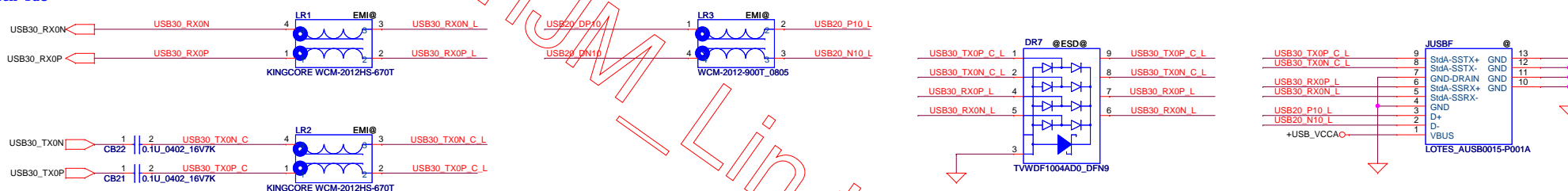
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

USB Sleep & Charge

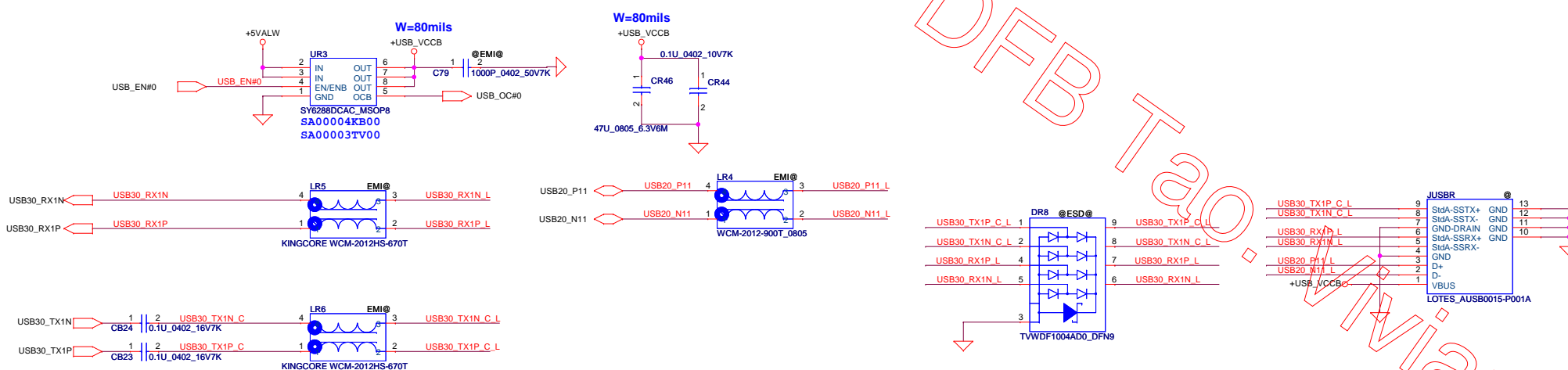
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode. DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



Front with S&C



Rear

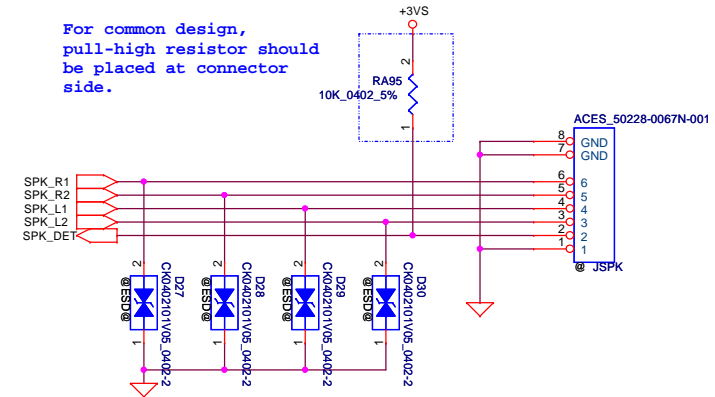


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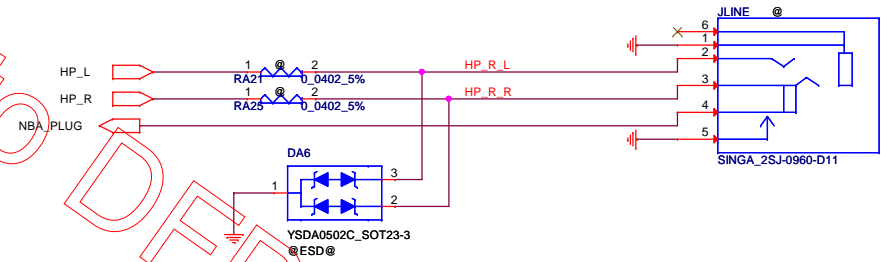
SPK CONN.

Non-Harman detection		
SPK_DET0	0	ONKYO
	1	Non-Brand

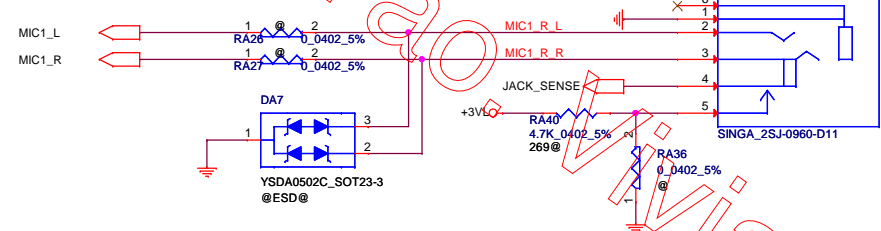
Please check SPK_DET pull high 10K to +3VS



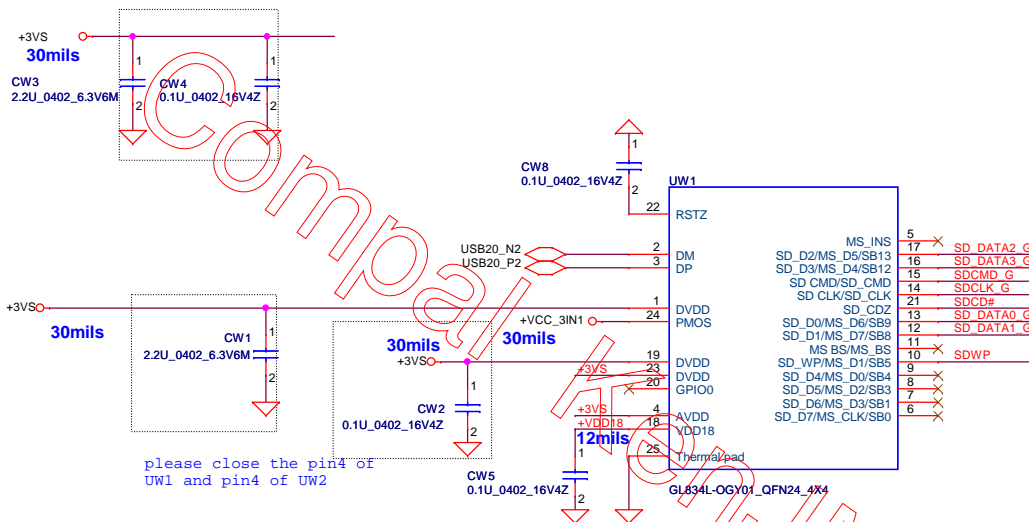
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

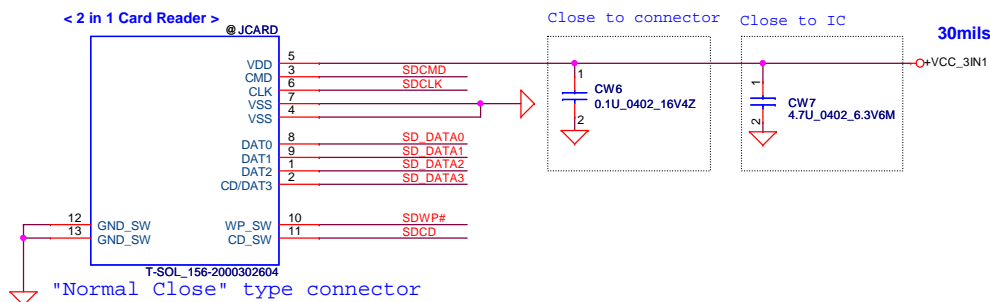


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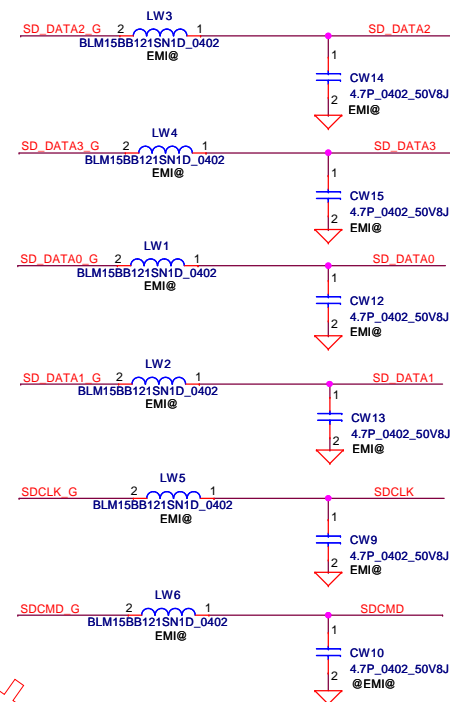


	NC (default)	10K pull down
GPI00	Power saving mode	Normal mode

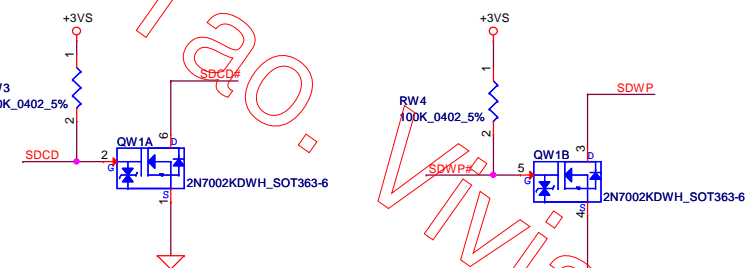
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



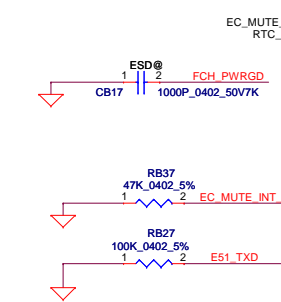
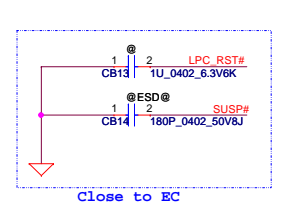
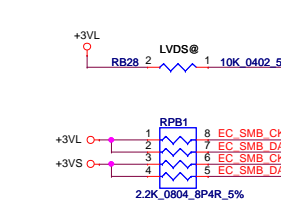
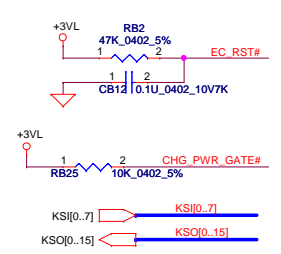
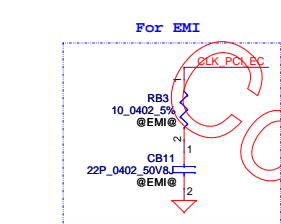
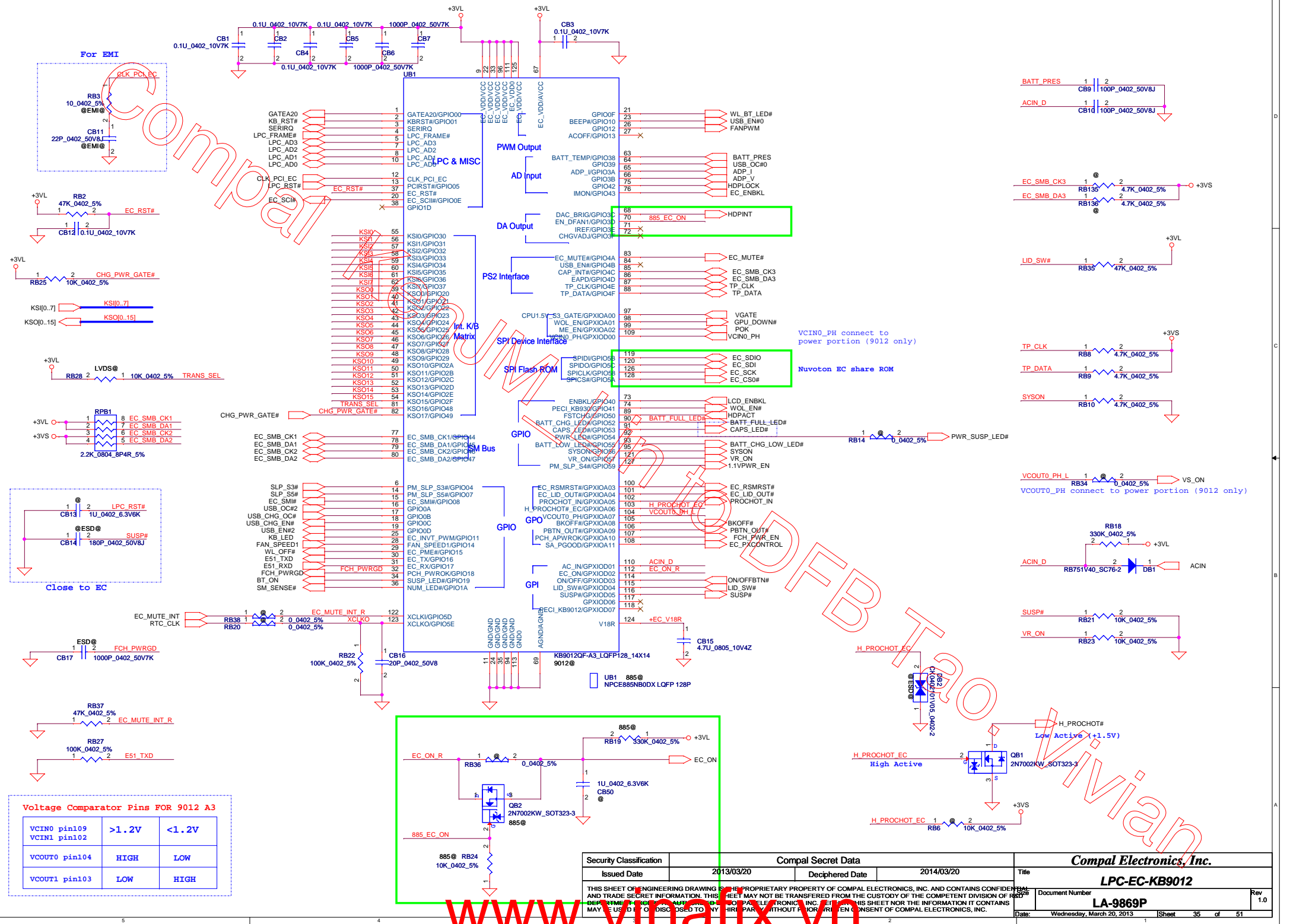
	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close



For normal close type connector invert circuit

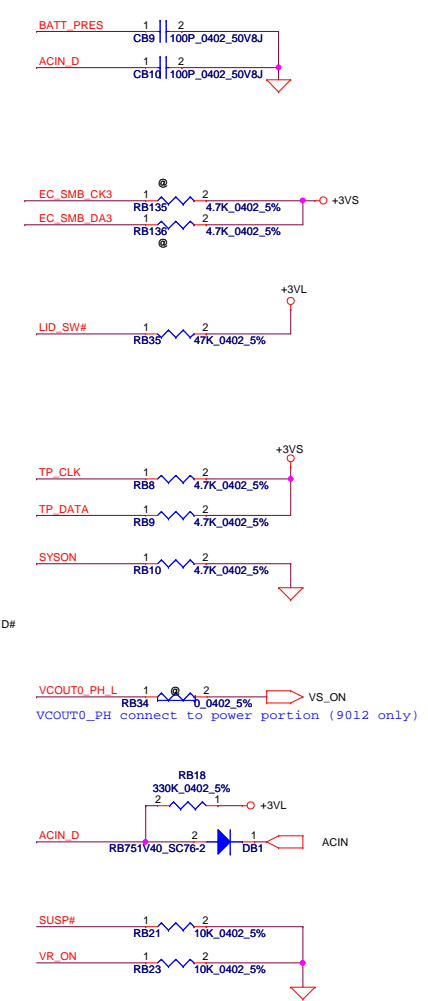
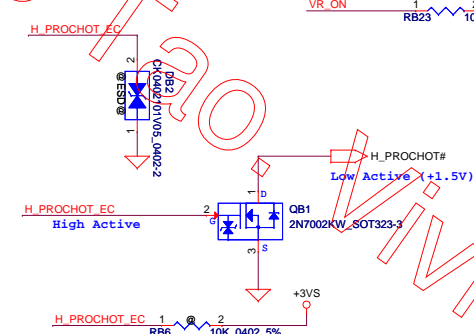
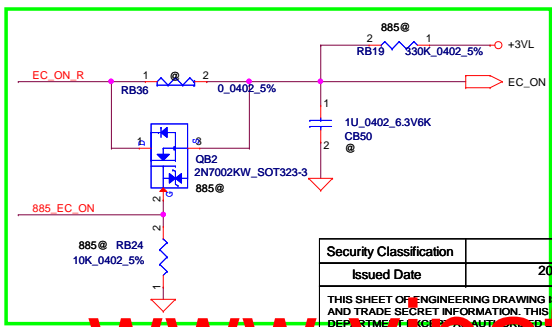


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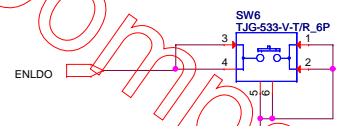


Voltage Comparator Pins FOR 9012 A3

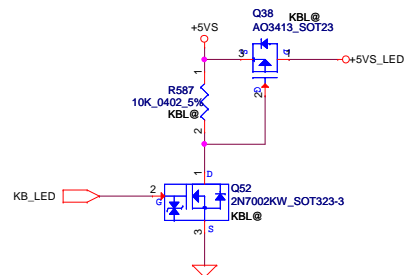
VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102	HIGH	LOW
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



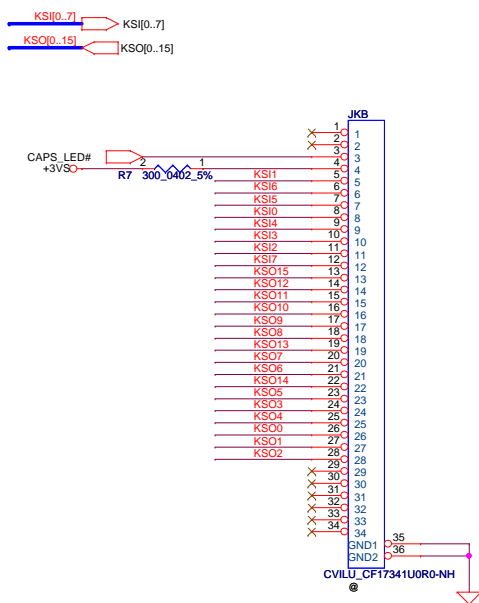
Battery Reset



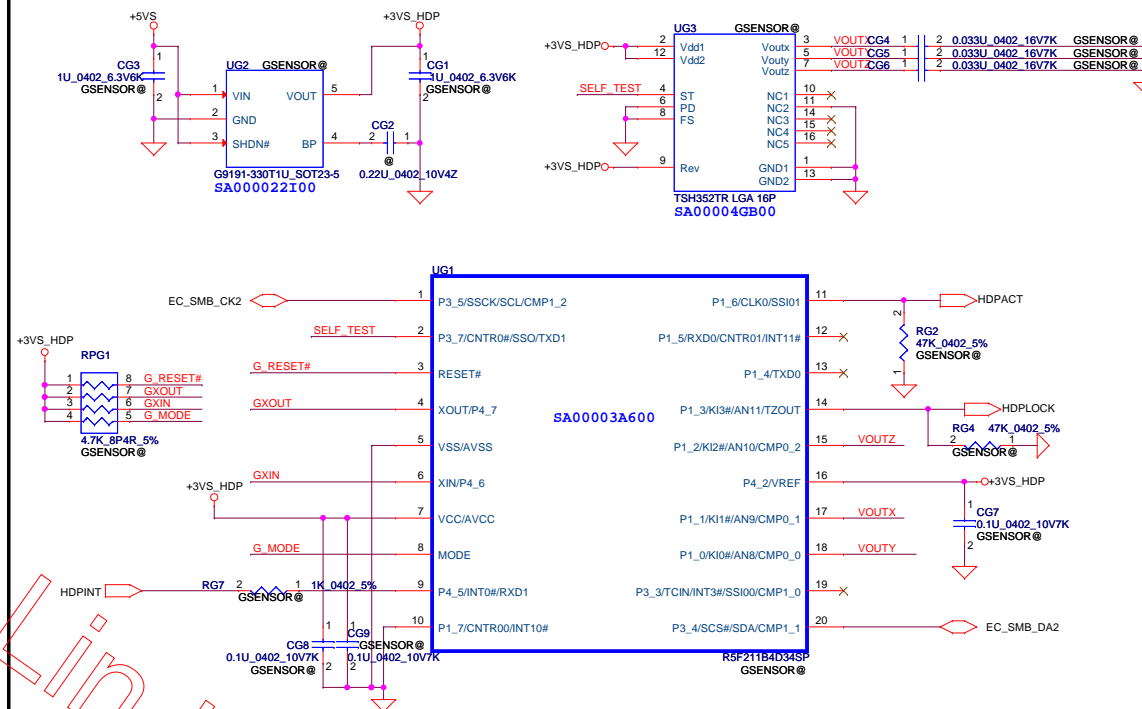
Keyboard LED



NEW KEYBOARD CONN.



G-SENSOR



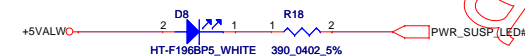
LED

BATT CHARGE(Blink) /FULL LED



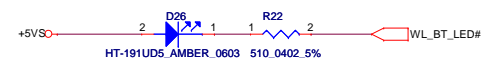
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED(Blink)



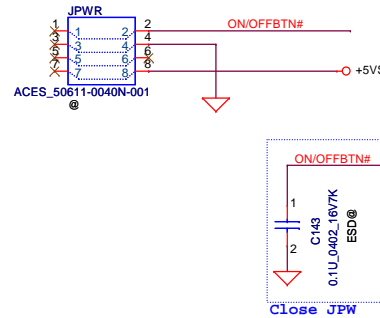
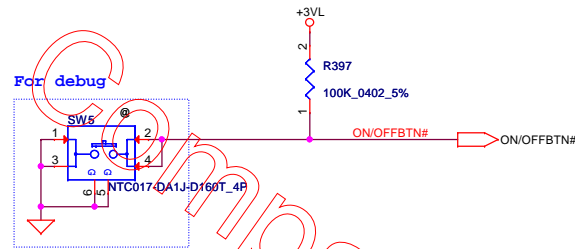
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN LED

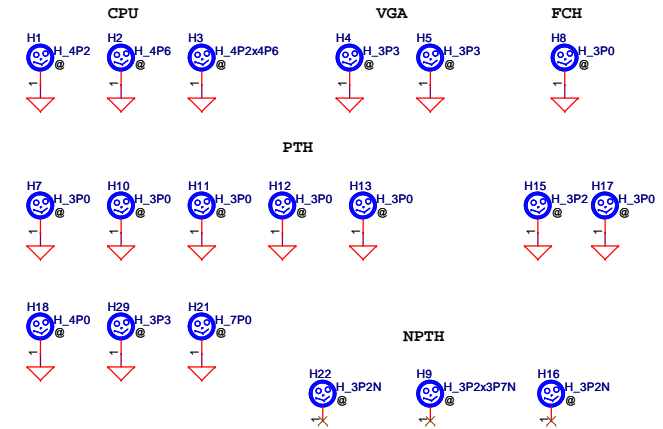


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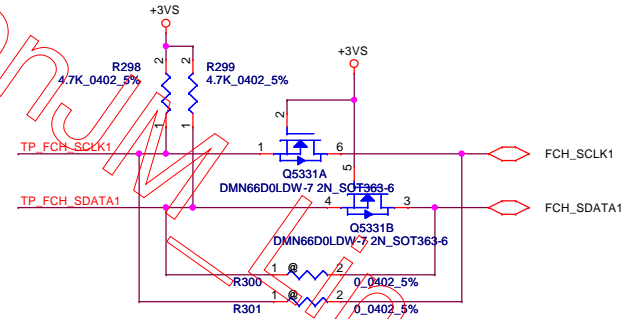
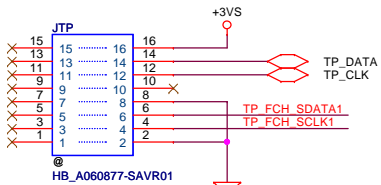
Conn.



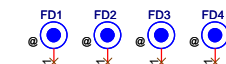
Screw Hole



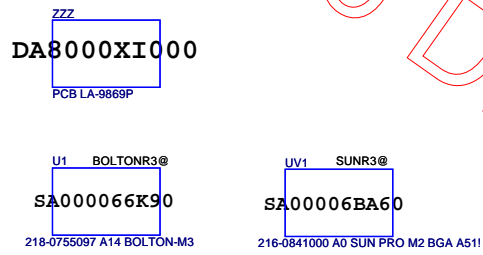
Touchpad Connector



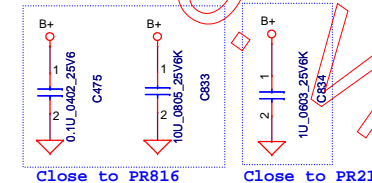
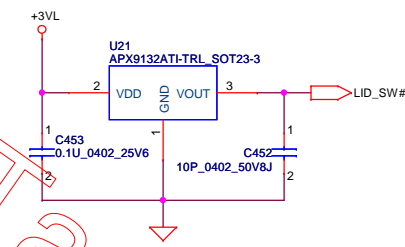
PCB Fedical Mark PAD



ISPD

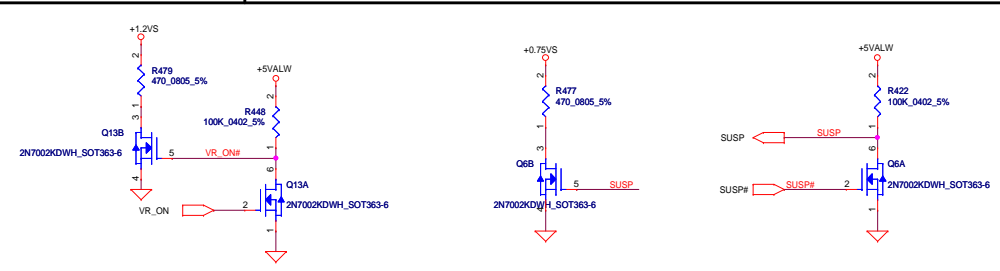
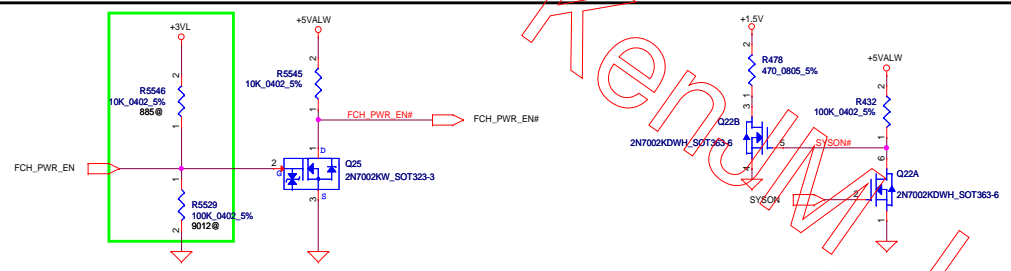
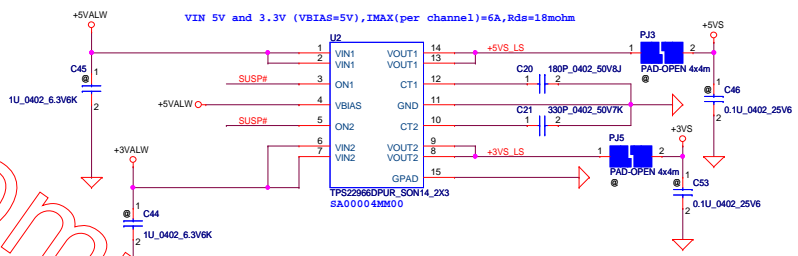


Lid SW

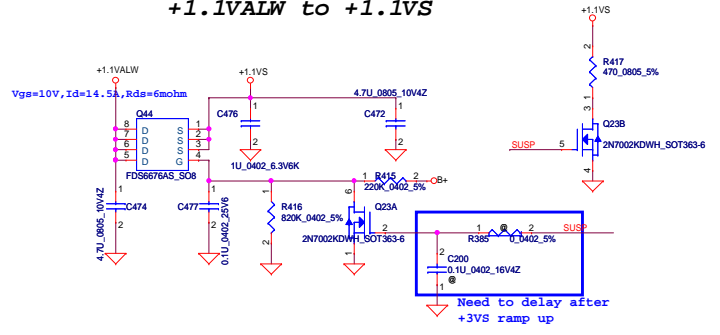


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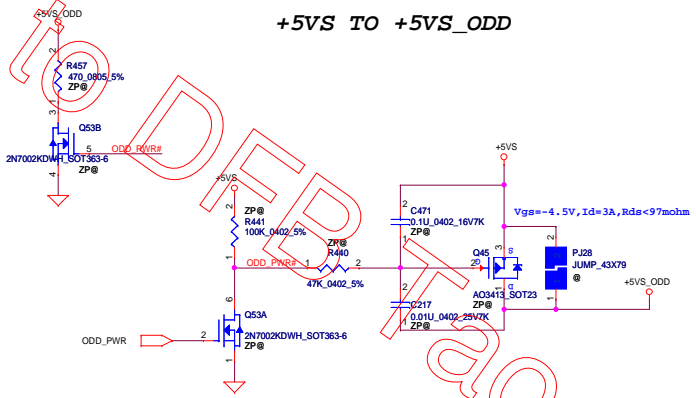
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



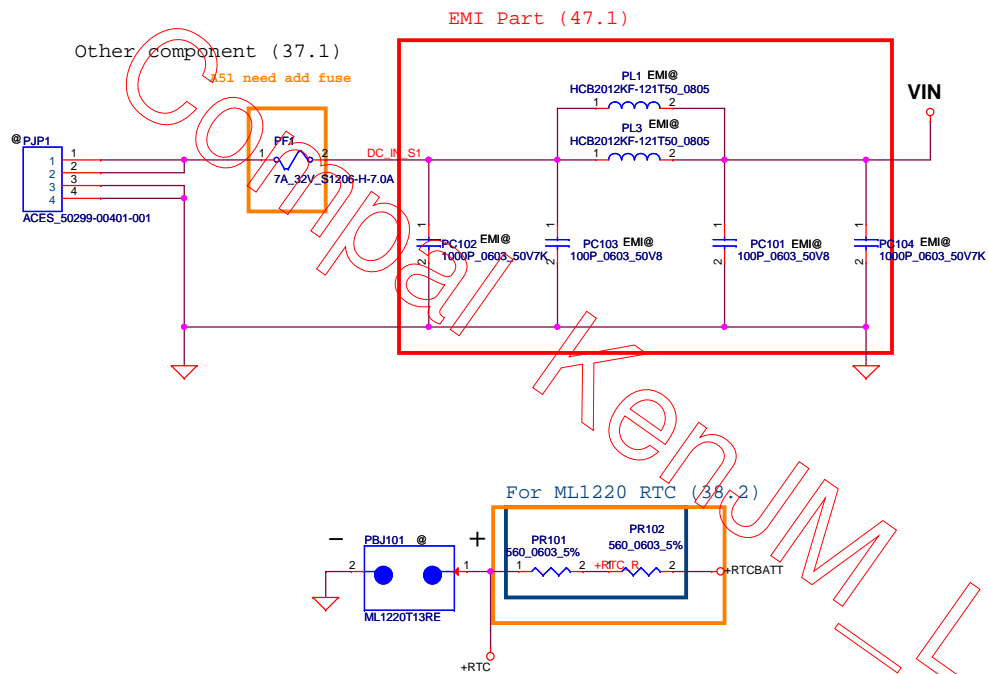
+1.1VALW to +1.1VS



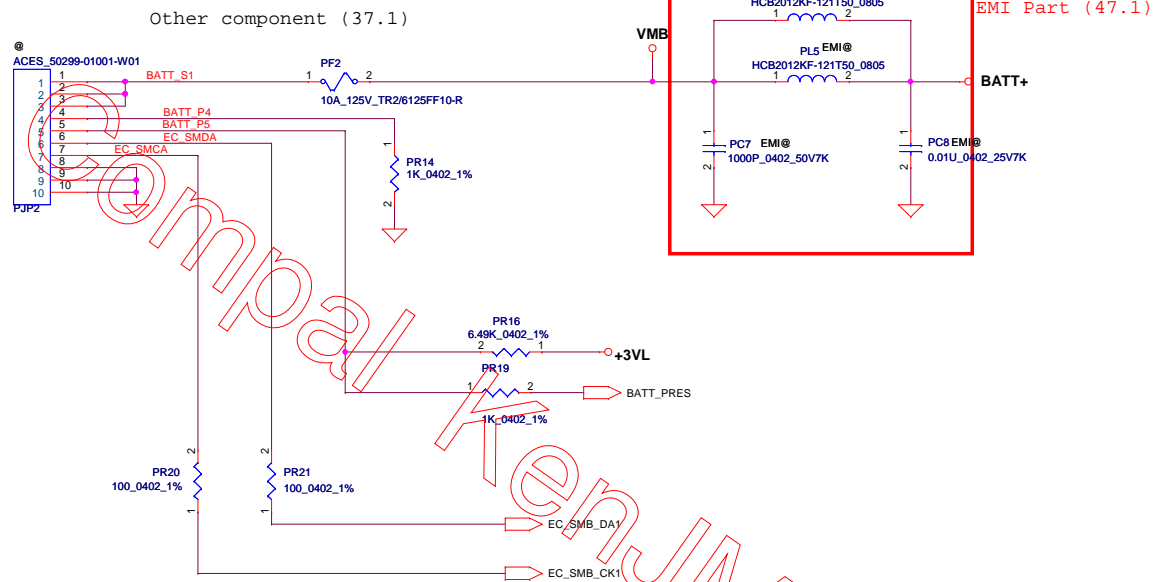
+5VS TO +5VS_ODD



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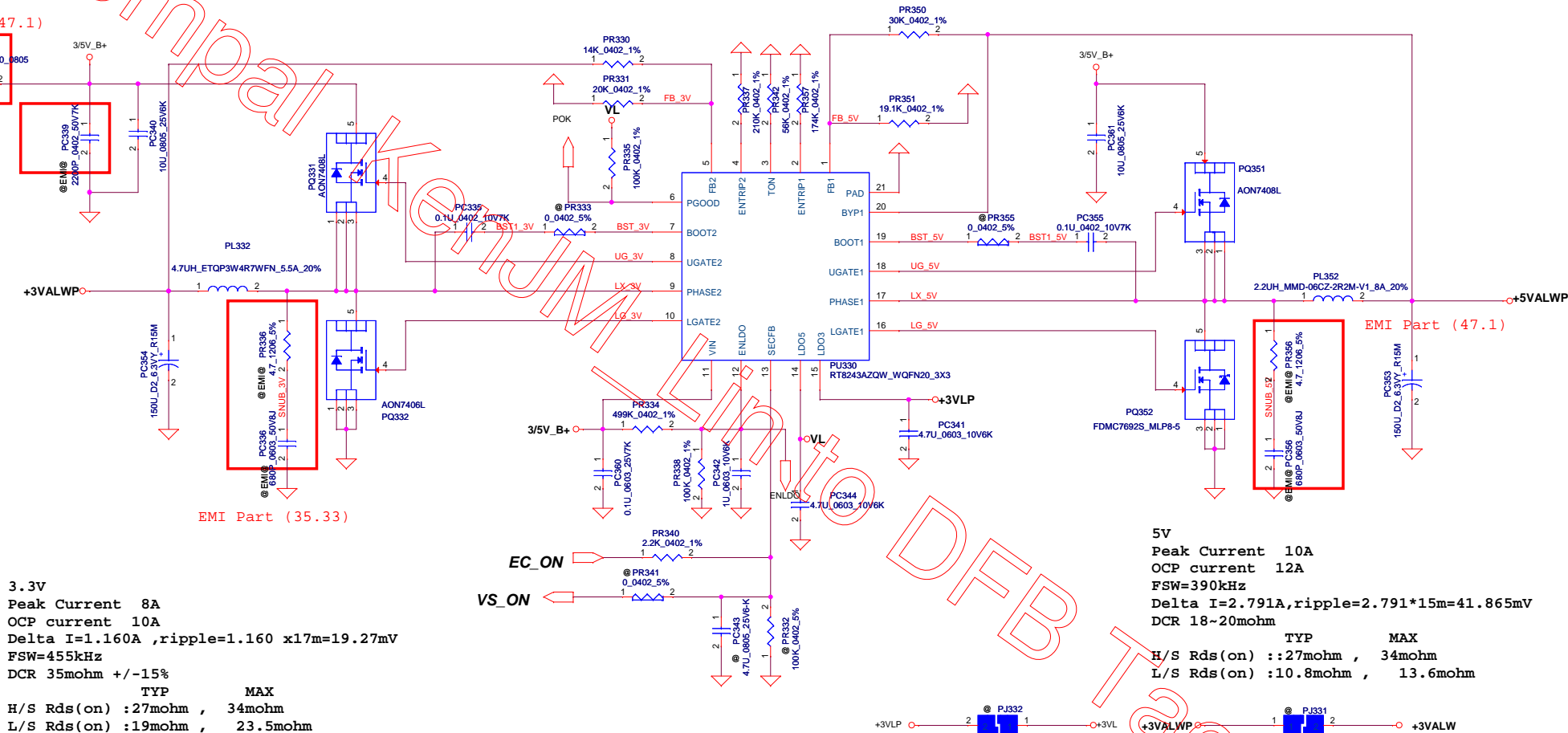


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Date:				Rev 1.0
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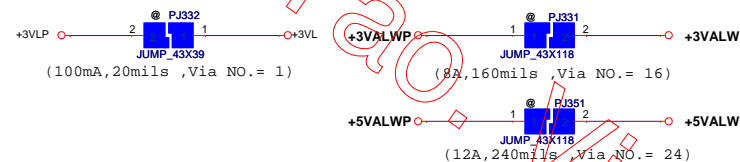
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EMI Part (47.1)

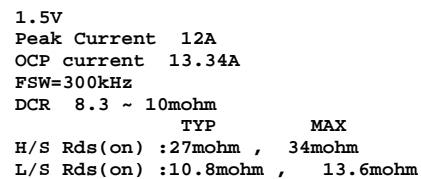


EMI Part (35.33)

EMI Part (47.1)



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						3VALW/5VALW
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Custom						1.
Date		Sheet		42		of 51



Note: S3 - sleep ; S5 - power off

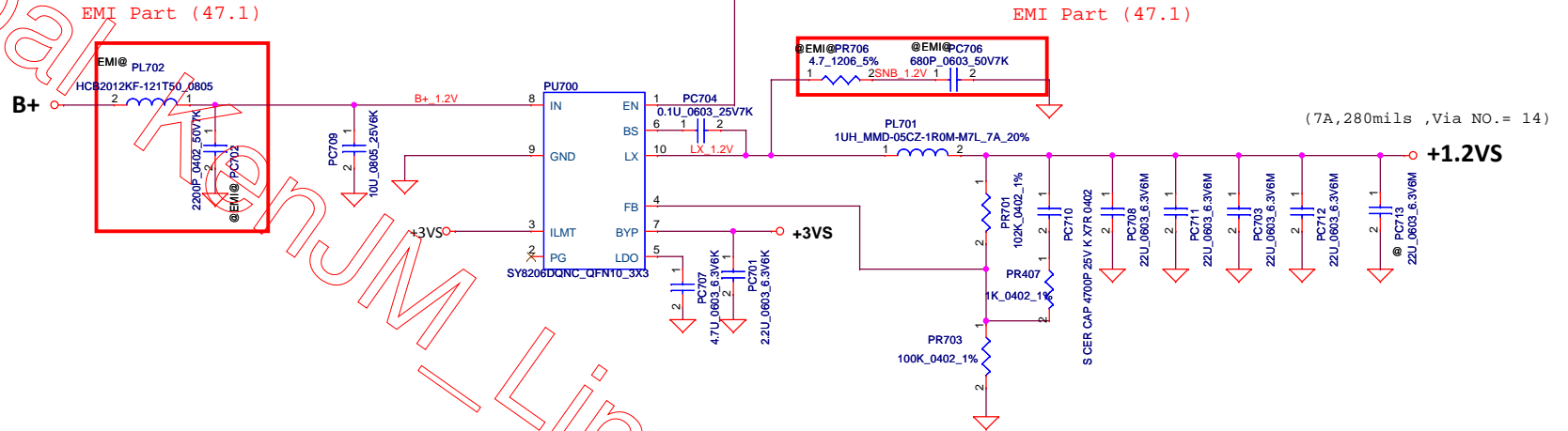
www.vinalix.vn

[illegible]

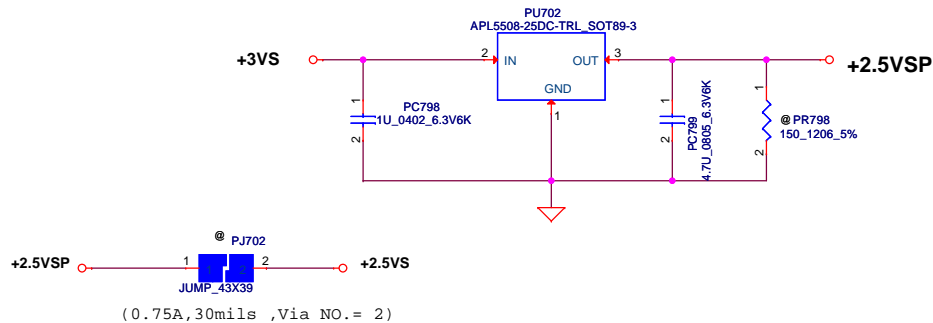
1.2V controller (35.7), Support component (35.8)

1.2V
Peak Current 7A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,



2.5V controller (35.13), Support component (35.14)



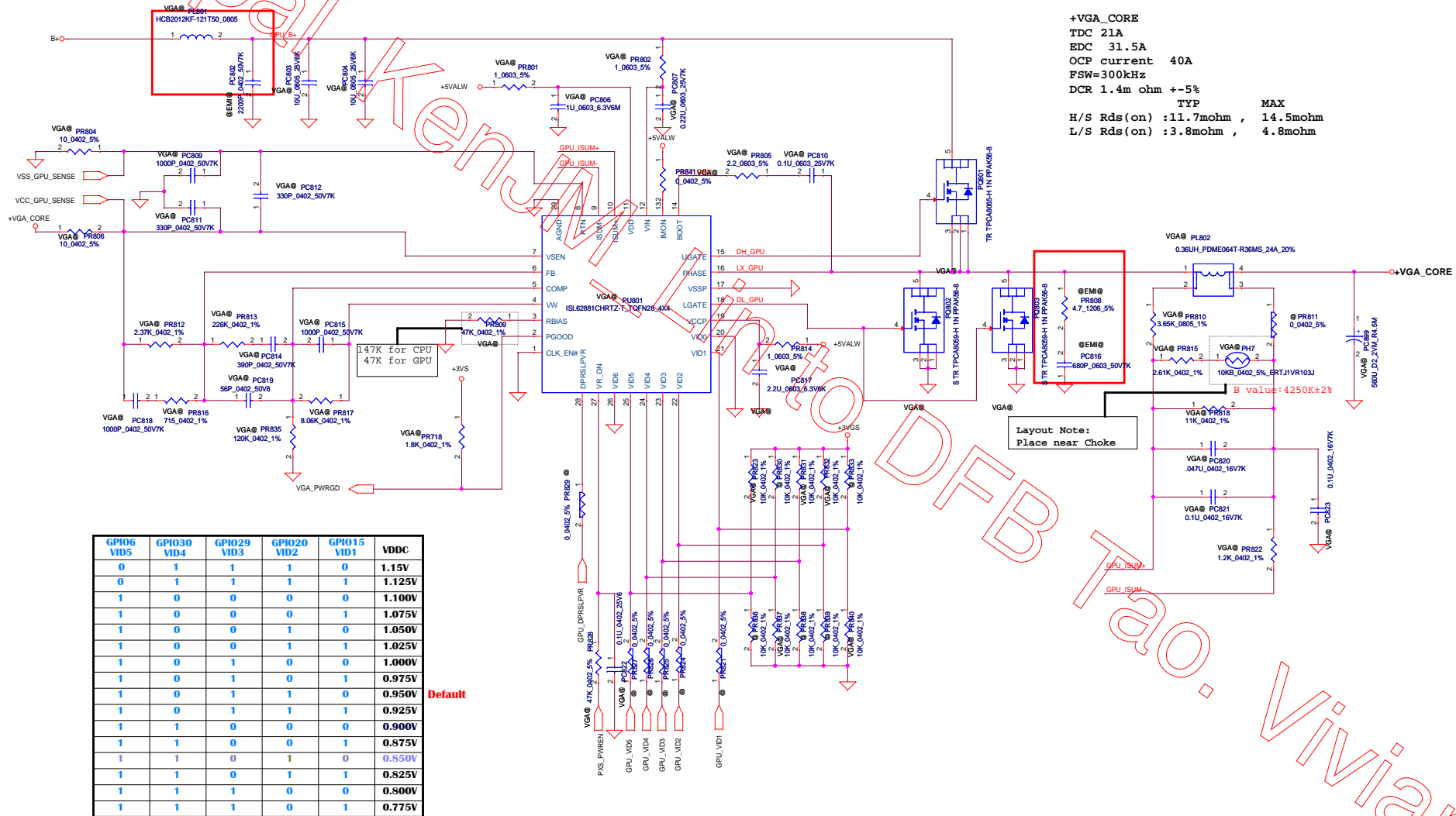
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				+1.2VSP/+2.5VSP			
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VGA controller (43.1),Driver (43.2) Support component (43.3)

EMI Part (47.1)

+VGA_CORE
TDC 21A
EDC 31.5A
OCP current 40A
FSW=300kHz
DCR 1.4m ohm +-5%
TYP MAX
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :3.8mohm , 4.8mohm



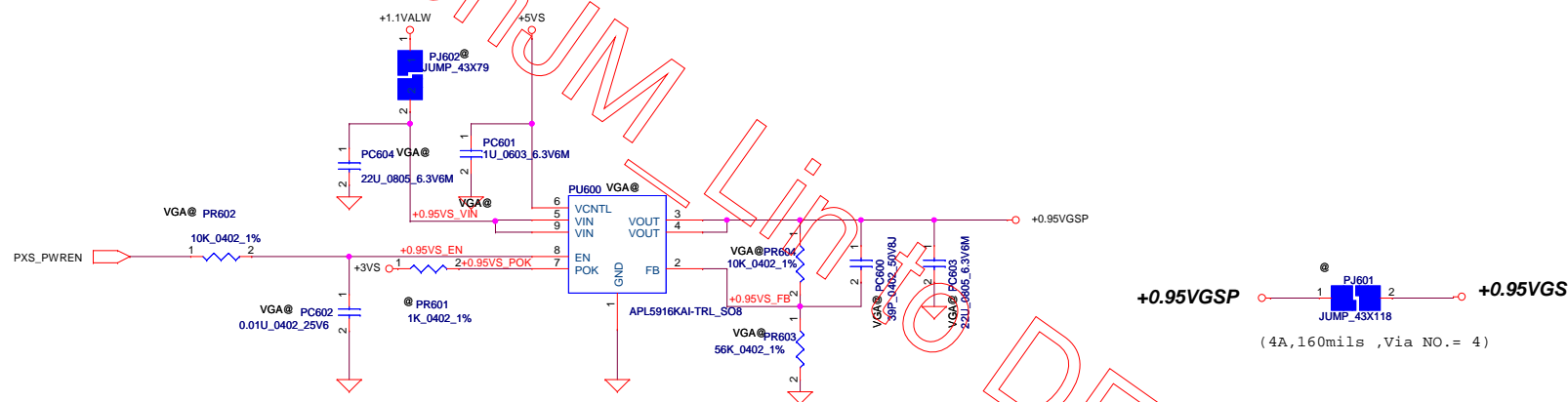
GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	1	0	0	0	0.925V
1	1	0	0	1	0.900V
1	1	0	0	1	0.875V
1	1	0	1	1	0.850V
1	1	1	0	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

Layout Note:
Place near Choke

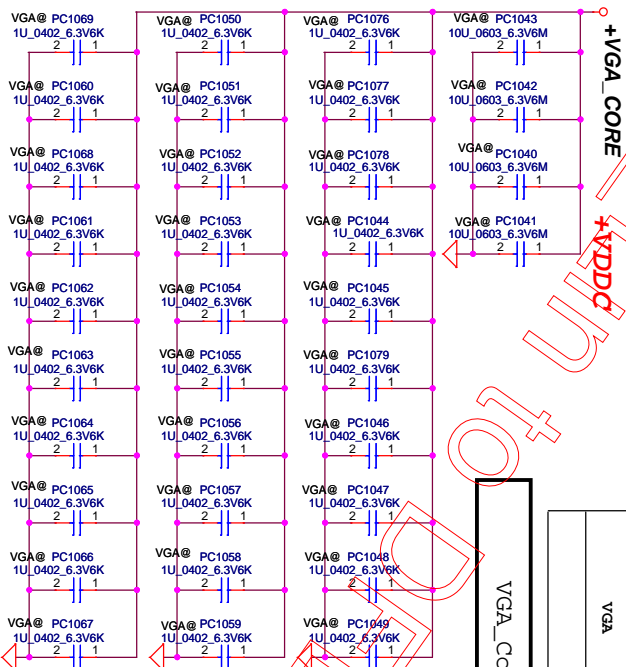
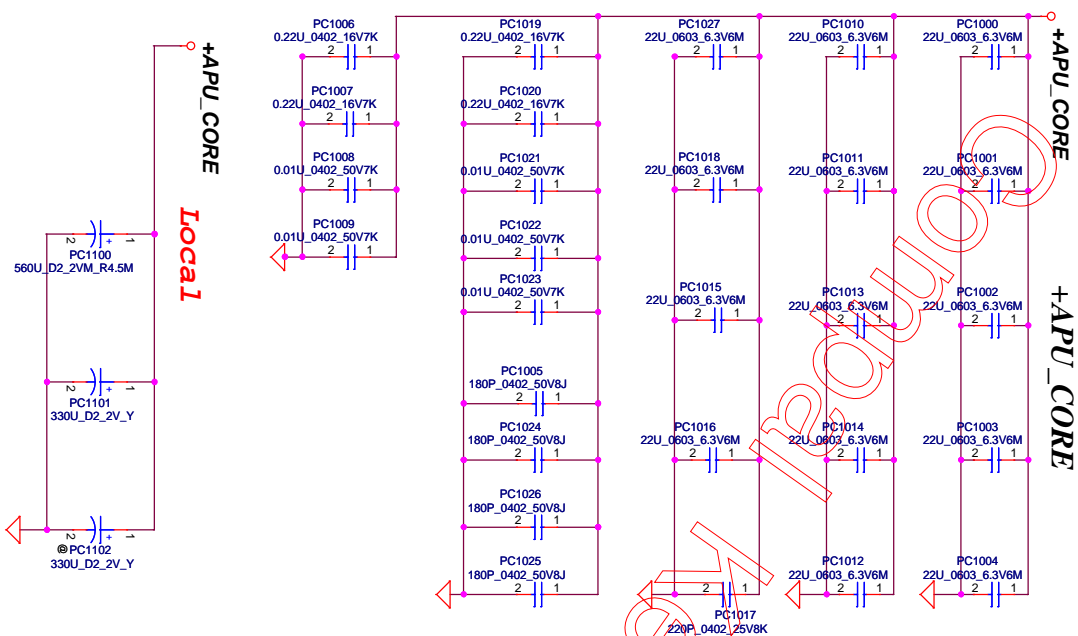
B value:4250K±2%

0.95V controller (35.11), Support component (35.12)



0.95V
Peak Current 4A
OCP current 16A
FSW=800kHz
H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

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				+1.5VPCIE/0.935V				
				Size		Document Number		Rev
				LA-9869P				1.0
				Date:		Wednesday, March 20, 2013		Sheet 48 of 51

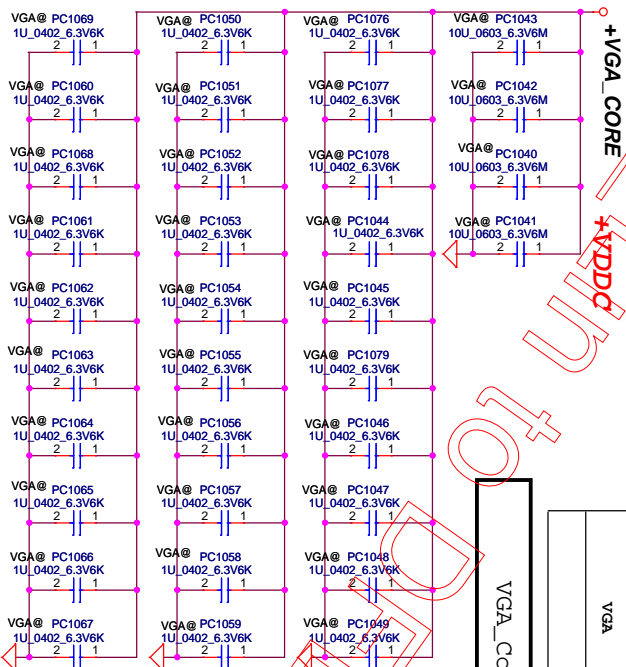


GFX output CAP (Including MLCC) 36.5

Richland	330uF*9m	22uF	0.01u	0.22uF	180P
VDD	4	1.5	5	4	4
VDD_NB	1	4	2	3	

VGA	560u x1	10u x 4	1u x30
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VGA_Core output CAP (Including MLCC 43.9)



Item	Reason for change	PG#	Modify List	Date	Phase
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Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT-2012/11/28	P39-PWR-BATTERY CONN / OTP	change PF2 vendor for cost down plane	PWR
2	EVT-2012/11/28	P41-PWR-+3VALW/5VALW	change PR337 235K to 210K & PR5357 156k to 174k	PWR
3	EVT-2012/11/28	P41-PWR-+3VALW/5VALW	Delate PC351 add PC353 150u D2 cap	PWR
4	EVT-2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PC157 220u H=4.5mm to 330u D2 cap H=2mm	PWR
5	EVT-2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PR158 16.2K to 17.4K	PWR
6	EVT-2012/11/28	P50-PWR-CPU_CORE	change the PC1101 560u to 330u	PWR

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Issued Date	2013/03/20	Deciphered Date	2014/03/20	Title	PIR (PWR)
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HW PIR (Product Improve Record)

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

GERBER-OUT DATE: 2012/12/25

Item	Page	Date	Request	Solution
1)	21	2012/12/04a	For CRT undershoot issue	Add R66 & R67 for CRT issue.
2)	14	2012/12/04a	For VGA_CORE display	unomunt CR103.
3)	22	2012/12/13a	For EMI request	Change L8/L9/L10/L11 part number for EMI request.
4)	34	2012/12/13a	For change EC PIN	Change 1.1VPWR_EN from pin 71 to pin 127 and USB_EN#0 from pin84 to pin 23.
5)	19	2012/12/14a	For LVDS translator	Delete all of RTD2132S components.
6)	31	2012/12/14a	For S&C port wake	Add CHG_PWR_GATE# on U15 pin 1 and connect to EC pin82.
7)	24	2012/12/17a	For leakage with PXS_PWREN	Change Power rail from +3VALW_FCH to +3VALW on R216 pin1
8)	07	2012/12/22a	For leakage	Delete R47, D18.
9)	24	2012/12/22a	For NV suggestion	Add R283 & Q30.
10)	34	2012/12/25a	For S&C port wake	Add RB25.

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3

GERBER-OUT DATE: 2013/02/04

Item	Page	Date	Request	Solution
1)	24	2013/01/21a	For AMD suggestion	Update R288/R289 from 10K to 2.2K.
2)	22	2013/01/21a	For HDMIleakage issue	Change R571 to +3VS power rail.
3)	34	2013/01/21a	For Audio noise	Add EC MUTE_INT (GPIO5D) and add RB38(0 ohm) and RB37 (4.7K PD)
4)	20	2013/01/21a	For layout routing	SWAP L56.
5)	20	2013/01/21a	For EMI request	Add R155/156
6)	13	2013/01/28a	For Safety	Add GPU_DOWNS connect to EC.
7)	25	2013/01/29a	For EMI request	Add C588(10p)/R118(0 ohm) with FCH_SPI_CLK_R.
8)	33	2013/01/30a	For ESD request	Reserve D27-D30 on SPK.
9)	07	2013/01/30a	For ESD request	Reserve D31 on APU_PROCHOT#.
10)	20	2013/01/30a	For ESD request	Add D32 on Int mic clk/data and USB.
11)	34	2013/01/30a	For ESD request	Reserve DB2 on H_PROCHOT_EC.
12)	36	2013/01/31a	For move JTP	SWAP JTP
13)	24	2013/02/01a	For ESD request	Add 1000p C505 on FCH_PWRGD.
14)	34	2013/02/01a	For ESD request	Add 1000p CB17 on FCH_PWRGD.
15)	34	2013/02/04a	For PWR	Add GPIO pin 99 of EC for power.